SIEMENS

Hand Book 1974

LSL
Low-speed logic
Characteristics · applications

SIEMENS

LSL
Low-speed logik

Hand Book 1974

SIEMENS AKTIENGESELLSCHAFT

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General Information

contained in Data Book 1974/75, volume 1, German edition
(Order No. B12/1201)

1. TTL Series FL 100–7400

With exception of the following types FLJ 331, FLJ 471, 74278, 74279, 74284, 74285, 74298, FLJ 101, FLQ 141, FLR 111, FLR 121, FLR 151, series FL 100 can also be supplied in temperature range 5.

FLH 101	7400	Quadruple 2-input NAND-gate
FLH 111	7410	Triple 3-input NAND-gate
FLH 121	7420	Dual 4-input NAND-gate
FLH 131	7430	8-input NAND-gate
FLH 141	7440	Dual 4-input NAND-powergate
FLH 151	7450	Dual 2+2-input AND/OR-gate, inverting with expander node
FLH 161	7451	Dual 2+2-input AND/OR-gate, inverting
FLH 171	7453	2+2+2+2-input AND/OR-gate, inverting with expander
FLH 181	7454	2+2+2+2-input AND/OR-gate, inverting
FLH 191	7402	Quadruple 2-input NOR-gate
FLH 191 S	7402 S1	as FLH 191/195, however output 6.5 V/500 µA
FLH 201	7401	Quadruple 2-input NAND-gate with open collector output
FLH 201 S	7401 S1	as FLH 201/205, however output 15 V/250 µA
FLH 201 T	7401 S3	as FLH 201/205, however output 5.5 V/50 µA
FLH 211	7404	Hexinverter
FLH 221	7480	1 bit fulladder
FLH 231	7482	2 bit fulladder
FLH 241	7483	4 bit fulladder
FLH 251	4929	Dual 2-input NAND-gate and quadruble inverter
FLH 271	7405	Hexinverter with open collector output
FLH 271 S	7405 S1	as FLH 271/275, however output 15 V/250 µA
FLH 271 T	7405 S3	as FLH 271/275, however output 5.5 V/50 µA
FLH 281	7442	BCD-decimal decoder
FLH 291	7403	Quadruple 2-input NAND-gate with open collector output
FLH 291 S	7403 S1	as FLH 291/295, however output 15 V/250 µA
FLH 291 T	7403 S3	as FLH 291/295, however output 5.5 V/50 µA
FLH 291 U	7426	as FLH 291/295, however output 15 V/50 µA
FLH 321	4930	Quadruple 2-input NAND-powergate
FLH 331	4931	Dual 5-input NAND-gate
FLH 341	7486	Quadruple 2-input exclusive OR-gate
FLH 351	7413	Dual 4-input NAND-Schmitt Trigger
	7414	Hex NAND-Schmitt Trigger
FLH 361	7443	Excess 3-decimal decoder
FLH 371	7444	Excess 3-Gray-decimal decoder
FLH 381	7408	Quadruple 2-input AND-gate
FLH 391	7409	Quadruple 2-input AND-gate with open collector output
FLH 391 T	7409 S1	as FLH 391/395, however output 15 V/250 µA

FLH	401	74181	4 bit arithmetic logic unit (ALU)
FLH	411	74182	Lookahead carry generator for ALU
FLH	421	74180	8 bit parity generator
FLH	431	7485	4 bit comparator
FLH	441	74H 87	4 bit complement unit
FLH	451	74H 183	Dual 1 bit fulladder
FLH	461	4934	Hexinverter with expander node and open collector
FLH	471	4935	Hexinverter with expander node
FLH	481	7406	Hexinverter with open collector output with 30 V/40 mA
FLH	481 T	7416	Hexinverter with open collector output with 15 V/40 mA
FLH	491	7407	Hexbuffer with open collector output with 30 V/40 mA
FLH	491 T	7417	Hexbuffer with open collector output with 15 V/40 mA
FLH	501	7412	Triple 3-input NAND-gate with open collector output
FLH	511	7423	Dual 4-input NOR-gate with strobe and expander node
FLH	521	7425	Dual 4-input NOR-gate with strobe
FLH	531	7437	Quadruple 2-input NAND-powergate
FLH	541	7438	Quadruple 2-input NAND-powergate with open collector output
FLH	551	7448	BCD-7-segment decoder
FLH	561	74184	6 bit binary BCD converter
FLH	571	74185 A	6 bit binary BCD converter
FLH	601	74132	Quadruple 2-input NAND-Schmitt Trigger
FLH	611	7422	Dual 4-input NAND-gate with open collector output
FLH	621	7427	Triple 3-input NOR-gate
FLH	631	7432	Quadruple 2-input OR-gate
FLH	641	49703	Hex delay element
FLH	731	49713	Dual 3-input NAND-Schmitt Trigger with high input impedance
FLH	731	49713S1	Dual 3-input NAND-Schmitt Trigger with high input impedance
FLH	661	7428	Quadruple 2-input NOR-gate
		7433	Quadruple 2-input NOR-gate with open collector
		74128	Quadruple 2-input NOR-buffer for 50-Ω-lines
		7483 A	4 bit fulladder
		74283	4 bit fulladder
		74125	Quadruple 1-input AND-gate with control input and tri-state output
		74126	Quadruple 1-input AND-gate with control input and tri-state output
		74136	Quadruple 2-input exclusive OR-gate with open collector output
		74147	4 bit decimal BCD converter
		74148	3 bit decimal BCD converter
FLJ	101	7470	3+3-input JK flipflop
FLJ	111	7472	JK-Master-Slave flipflop
FLJ	121	7473	Dual JK-Master-Slave flipflop with reset
FLJ	131	7476	Dual JK-Master-Slave flipflop with set and reset
FLJ	141	7474	Dual D-flipflop

FLJ 151	7475	Quadruple D-flipflop
FLJ 161	7490 A	Decimal counter
FLJ 171	7492 A	Divide-by-twelve counter
FLJ 181	7493 A	4 bit binary counter
FLJ 191	7495 A	4 bit shiftregister, reversible
FLJ 201	74190	Reversible decimal counter
FLJ 211	74191	Reversible 4 bit binary counter
FLJ 221	7491 A	8 bit shiftregister, serial in/out
FLJ 231	7494	4 bit shiftregister, parallel in, serial out
FLJ 241	74192	Decimal counter with one clock input each for up and down count
FLJ 251	74193	4 bit binary counter with one clock input each for up and down count
FLJ 261	7496	5 bit shiftregister
FLJ 271	74107	Dual JK-Master-Slave flipflop
FLJ 281	74104	JK-Master-Slave flipflop with JK input
FLJ 291	74105	JK-Master-Slave flipflop with $\overline{J}$, $\overline{K}$ and JK inputs
FLJ 301	74100	Eight D flipflop
FLJ 311	74198	Universal 8 bit shiftregister, reversible
FLJ 321	74199	Universal 8 bit shiftregister
FLJ 331	7497	Programmable 6 bit rate multiplier
FLJ 341	74110	JK-Master-Slave flipflop with data lockout
FLJ 351	74111	Dual JK-Master-Slave flipflop with data lockout
FLJ 361	74118	Hex RS-flipflop with common reset
FLJ 371	74119	Hex RS-flipflop with separate reset
FLJ 381	74196	Decimal counter for 50 MHz
FLJ 391	74197	4 bit binary counter for 50 MHz
FLJ 401	74160	Synchronous decimal counter with set and reset
FLJ 411	74161	Synchronous 4 bit binary counter with set and reset
FLJ 421	74162	Fully synchronous decimal counter with set and reset
FLJ 431	74163	Fully synchronous 4 bit binary counter with set and reset
FLJ 441	74164	8 bit shiftregister, parallel out
FLJ 451	74165	8 bit shiftregister, parallel in
FLJ 461	74166	Universal 8 bit shiftregister
FLJ 471	74167	Programmable decimal rate multiplier
FLJ 481	4932	Dual 8 bit shiftregister
FLJ 491	49702	Quadruple D-flipflop with common reset
FLJ 501	49704	Dual 4 bit binary counter for 50 MHz
FLJ 511	49705	Dual decimal counter for 50 MHz
FLJ 521	74115	Dual JK-Master-Slave flipflop with data lockout
FLJ 531	74174	Hex D-flipflop with common reset
FLJ 541	74175	Quadruple D-flipflop with common reset
FLJ 551	74194	Synchronous 4 bit parallel shiftregister, reversible
FLJ 561	74195	Synchronous 4 bit parallel shiftregister with JK inputs
	74109	Dual JK flipflop with set and reset
	74173	Quadruple D-flipflop with tri-state output
	74176	Decimal counter for 35 MHz
	74177	4 bit binary counter for 35 MHz

	74178	4 bit parallel shiftregister
	74179	4 bit parallel shiftregister
	74278	4 bit priority register
	74279	Quadruple RS-flipflop with separate reset inputs
	74298	Quadruple 2 bit dataselector with memory
FLK 101	74121	Monostable multivibrator
FLK 111	74122	Monostable multivibrator with reset
FLK 121	74123	Dual monostable multivibrator with reset
FLL 101	74141	BCD-decimal decoder-driver for indicator tubes
FLL 111	7445	BCD-decimal decoder-driver with open collector outputs
FLL 111 T	74145	as FLL 111, however outputs 15 V/80 mA
FLL 121	7446	BCD-7-segment decoder-driver with open collector outputs with 30 V/20 mA
FLL 121 T	7447	as FLL 121, however outputs 15 V/20 mA
FLL 121 U	7446 A	as FLL 121, however outputs 30 V/40 mA
FLL 121 V	7447 A	as FLL 121, however outputs 15 V/40 mA .
FLL 131	49700	Dual AND-powerdriver for 30 V/160 mA and dual 2-input NAND-gate
FLL 131 T	49700S1	as FLL 131, however outputs 60 V/160 mA
FLL 141	49701	Quadruple powerdriver for 30 V/80 mA
FLL 141 T	49701S1	as FLL 141, however outputs 60 V/80 mA
FLL 151	74142	Decimal counter, latch, decoder and driver for indicator tubes
FLL 171	74143	4 bit binary counter, latch 7-segment decoder and driver
FLL 171T	74144	4 bit binary counter, latch 7-segment decoder and driver
FLQ 101	7489	64 bit random access memory
FLQ 111	7481 A	16 bit random access memory
FLQ 121	7484 A	16 bit random access memory
FLQ 131	74170	16 bit random access memory, 4 words of 4 bits
FLQ 141		256 bit random access memory with tristate outputs
	74172	16 bit random access memory
FLR 101	7488 A	256 bit read-only memory
FLR 111	74187	1024 bit read-only memory
FLR 121		Programmable 256 bit read-only memory
FLR 131		Programmable 1024 bit read-only memory
FLY 101	7460	Expander for FLH 151, FLH 171 and FLH 511
FLY 111	74150	16 bit data selector/multiplexer
FLY 121	74151	8 bit data selector/multiplexer
FLY 131	74153	Dual 4 bit data selector/multiplexer
FLY 141	74154	4 bit binary decoder/multiplexer
FLY 151	74155	Dual 2 bit binary decoder/demultiplexer
FLY 161	74156	Dual 2 bit binary decoder/demultiplexer with open collector outputs
FLY 171	74157	Quadruple 2 bit data selector/multiplexer
FLY 181	74120	Dual pulse synchroniziser
	74284	Dual 4 bit parallel multiplier
	74285	Dual 4 bit parallel multiplier

2. LSL-Series FZ 100

3. MOS-Series

FDN141 A Programmable dynamic 256-bit-shiftregister with two clock inputs

FDN151 A Programmable dynamic 256-bit shiftregister with one clock input

GDR101
GDR106 2048-(2240-, 2304) bit-ROM

SAB 1000 Remole-control-transmitter*
SAB 1001 Remole-control-receiver*
SAB 1002 Remole-control-analogue-memory*

SAJ 131
SAJ 135 Static frequency divider 1000:1

SAJ 131 A
SAJ 135 A Static frequency divider 1000:1 with external reset input

SAJ 131 I
SAJ 135 I Static frequency divider 1000:1

SAJ 131 AI
SAJ 135 AI Static frequency divider 1000:1 with external reset input

SAJ 205 Sawtooth stearcase generator*
SAJ 341 Counter/clock-circuit*

SAJ 410 7-stage frequency divider

4. Spezial circuits

SAS 201, SAS 211 Magnetically controlled switches

*Information on request

Summary of Analog Integrated Circuits

contained in Datenbuch 1974/75, Band 2, German edition
(Order No. B 12/1213),
contained in Data Book 1974/75, English edition
(Order No. 12/1213.101)

Analog Integrated Circuits for Entertainment Applications

TAA 131	Three-stage AF amplifier
TAA 630 S	Synchronous demodulator for colour difference drive
TAA 991 D	AM/FM IF amplifier (DIL package, 14 pins)
TAA 991 Q	AM/FM IF amplifier (QIL package, 14 pins)
TBA 120	FM IF amplifier with demodulator (DIL package, 14 pins)
TBA 120 A	FM IF amplifier with demodulator (QIL package, 14 pins)
TBA 120 S	FM IF amplifier with demodulator (DIL package, 14 pins)
TBA 120 AS	FM IF amplifier with demodulator (QIL package, 14 pins)
TBA 120 T	FM IF amplifier with demodulator (DIL package, 14 pins)
TBA 120 U	FM IF amplifier with demodulator (DIL package, 14 pins)
TBA 400	Gain-controlled broadband amplifier (Package 5J10 DIN 41873)
TBA 400 D	Gain-controlled broadband amplifier (DIL package, 14 pins)
TBA 440 C	Gain-controlled video IF amplifier with demodulator (DIL package, 16 pins)
■ TBA 440 P	Video IF IC for black/white and colour TV sets (Control for pnp tuner prestages) (DIL 16)
TBA 440 N	Video IF IC for black/white and colour TV sets (Control for npn tuner prestages) (DIL 16)
TBA 450 N	Stereo decoder (DIL package, 16 pins)
TBA 460	AM/FM IF and AF amplifier (DIL package, 16 pins)
TBA 460 Q	AM/FM IF and AF amplifier (QIL package, 16 pins)
TBA 500 P	Luminance combination (voltage is positive going)
TBA 500 N	Luminance combination (voltage is negative going)
TBA 510	Chrominance combination
TBA 520	Colour demodulator
TBA 530	R.G.B. Matrix pre-amplifier
TBA 540	Reference combination
TBA 560 C	Luminance and chrominance control combination
TBA 920	Horizontal combination
TBA 970	Video amplifier
TCA 440	AM receiver circuit
TCA 890	AFT IC with automatic muting during tuning and incorporated 30 V reference voltage
■ SAS 560, SAS 570	Switching amplifier for 4-channel touch tuning
SAS 560 S/570 S	Switching amplifier for 4-channel touch tuning
SAS 580, SAS 590	Switching amplifier for 4-channel touch tuning
S 041 E, S 041 P	FM IF amplifier with demodulator
S 042 E, S 042 P	Mixer
UAA 170	IC for driving LED display line

Analog Integrated Circuits for Industrial Applications

TAA 521, TAA 521 A, TAA 522	operational amplifiers
TAA 721, TAA 722	broadband amplifiers
TAA 761, TAA 761 A, TAA 761 W,	operational amplifiers
TAA 765, TAA 765 A, TAA 765 W	operational amplifiers
TAA 762	operational amplifiers
TAA 861, TAA 861 A, TAA 861 W,	operational amplifiers
TAA 865, TAA 865 A, TAA 865 W	operational amplifiers
~~TAA 862, TAA 862 F~~	operational amplifiers
TBA 221, TBA 221 A, TBA 221 B,	operational amplifiers
TBA 221 W, TBA 222	operational amplifiers
TBA 830 G, TBA 830 R	microphone amplifiers
TCA 105, TCA 105 B, TCA 105 W, TCA 105 BW,	threshold switches
TCA 315 A	operational amplifier with Darlington input
TCA 325 A	operational amplifier
TCA 335 A	operational amplifier with Darlington input
TCA 345 A	threshold switches
S 0255	motor speed regulator
TCA 671	transistor array
TCA 871	transistor array
P 1	active matrix point

■ Not for new development

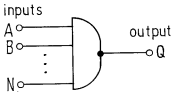
Logic Data and Symbols

1. Logic Levels

According to DIN 41785, sheet 4 for digital microcircuits the two possible values of binary electrical digits are given by L (Low) and H (High). The values of the L-range are defined as closer to $-\infty$, and the values of the H-range as closer to $+\infty$.
The logic symbols 0 and 1, or O and L, or log. 1 and log. 0 as well as positive or negative logic definitions are not used any longer.

2. Gate Symbols

2.1 NAND-Gate

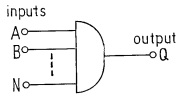


Truth table for a 2-input NAND-gate
(e. g. 1/4 FZH 101)

inputs A	B	output Q
L	L	H
L	H	H
H	L	H
H	H	L

Logic function: $Q = \overline{AB \ldots . N}$
Definition: An output signal will be present unless A and B and .... and N are present.

2.2 AND-Gate

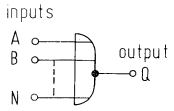


Truth table for a 2-input AND-gate
(e. g. 1/4 FZH 251)

inputs A	B	output Q
L	L	L
L	H	L
H	L	L
H	H	H

Logic function: $Q = AB \ldots . N$
Definition: An output signal will be present if A and B and .... and N are present.

2.3 NOR-Gate

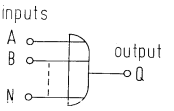


Truth table for a 2-input NOR-gate
(e. g. 1/4 FZH 281)

inputs A	inputs B	output Q
L	L	H
L	H	L
H	L	L
H	H	L

Logic function: $Q = \overline{A + B + ... + N}$
Definition: An output signal will be present if A or B or .... or N are not present.

2.4 OR-Gate

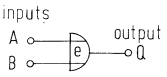


Truth table for a 2-input OR-gate
(e.g. 1/4 FZH 291)

inputs A	inputs B	output Q
L	L	L
L	H	H
H	L	H
H	H	H

Logic function: $Q = A + B + ... + N$
Definition: An output signal will be present if A or B or .... or N are present.

2.5 Exclusive-OR-Gate

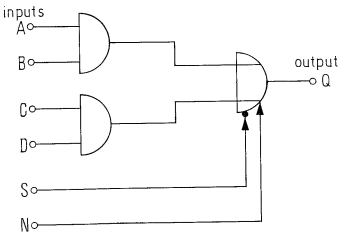


Truth table for a 2-input exclusive OR-gate
(e. g. 1/4 FZH 271)

inputs A	inputs B	output Q
L	L	L
L	H	H
H	L	H
H	H	L

Logic function: $Q = \overline{A}B + A\overline{B}$
Definition: An output signal will be present if only A or only B is present.

2.6 AND/OR-Gate



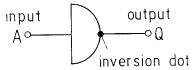
S = Strobe input
N = Delay input

Logic function: $Q = AB + CD$

Truth table for a 2 + 2-input AND/OR-gate (similator to 1/2 FZH 151)

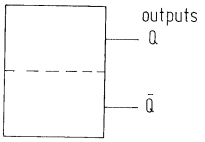
inputs A	B	C	D	output Q
L	L	L	L	L
H	L	L	L	L
L	H	L	L	L
H	H	L	L	H
L	L	H	L	L
H	L	H	L	L
L	H	H	L	L
H	H	H	L	H
L	L	L	H	L
H	L	L	H	L
L	H	L	H	L
H	H	L	H	H
L	L	H	H	H
H	L	H	H	H
L	H	H	H	H
H	H	H	H	H

2.7 Inverter

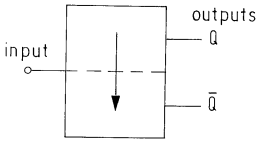


Logic function: $Q = \overline{A}$

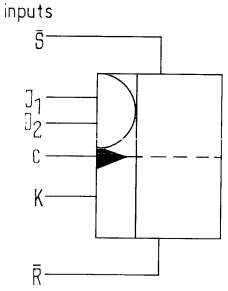
3. Flipflop Symbols



bistable circuit (flipflop) with complementary outputs

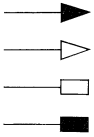


monostable circuit (monoflop) with an input acting upon both outputs. The arrow indicates the output which is high when the circuit is stable.



J_1 J_2 and K are information inputs
J_1 and J_2 are AND-connected
J and K-inputs are gated by clock input C
$\bar{R}$ and $\bar{S}$ are independent reset and set inputs

The arrow at the clock input shows the gating mode as follows:



action at the output occurs when the input rises from L to H
action at the output occurs when the input falls from H to L
action while the input is high
action while the input is low

4. Flipflop Classification according to the Logic Function

4.1 D-Flipflop (Delay-Flipflop)

The D-flipflop has an input (indicated with a D) the logic state of which is transferred into the flipflop. It is controlled by a clock pulse. The information stored during the clock pulse is retained until the next clock pulse. Only then any new information is accepted by the D-input.

4.2 JK-Flipflop

The JK-flipflop has information inputs indicated with a J and K. They are gated by the clock input and determine the output state Q of the flipflop.
At J = L and K = L the Q-output is retained in its original state. At J = H and K = H the flipflop switches at every clock pulse to its complementary state (binary divider). Q = L results at J = L and K = H independent of the preceding output state. For J = H and K = L the defined output state is Q = H.
Most JK-flipflops have additional $\overline{R}$ and $\overline{S}$ inputs with which the flipflop can be operated independent of the clock pulse. In this way it is possible to select the initial state of the flipflop. $\overline{R}$ and $\overline{S}$ indicates that set or reset action is at L-level only.
The following tables show the function of the different types of flipflops.

4.3 Truth Tables for Flipflops

inputs		output Q	
D or J	K	D-Flipflop	JK-Flipflop
L	L	L	Q_n
L	H		L
H	L	H	H
H	H		Q_n
t_n		t_{n-1}	

inputs		outputs	
$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
L	H	L	H
H	L	H	L
L	L	undefined	
H	H	Q_n	$\overline{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

Quality Levels

1. The quality of integrated circuits of the LSL-series is defined by the following statements:

1.1 Maximum ratings as well as upper and lower distribution boundary of typical characteristics.

1.2 Maximum amount of circuits which do not comply with the ratings given under 1.1. These acceptable quality levels or AQL-levels are based on final production testing in accordance with the AQL-table ABC-STD-105 D, inspection level II (see also paragraph II. 4).

2. Defects

A defect is indicated if an actual value measured does not correspond to the data sheet. The defects are classified into type and extent.

2.1 Type of defect
- A Mechanical defects of case and connections
- B Electrical defects

2.2 Extent of defect
- A Critical defects: any defect causing functional failure.
- B Gradual defects: defects which still permit functional applications.

3. The defects and the corresponding AQL-values are stated in the table below.

defect	AQL-levels for: LSL	note
3.1 Mechanical defect	0.65	1
A Critical defect	0.25	1
B Gradual defect	0.65	1
3.2 Electrical defects		
3.2.1 Static parameters of data sheet within the temperature range	1.0	1,3
A Critical defects	0.15	1
B Gradual defects	1.0	1
3.2.2 Switching parameters at 25 °C	1.5	2

Notes: 1 group-AQL = sum of defects of all parameters
2 AQL = defect of a single parameter
3 valid at 25 °C

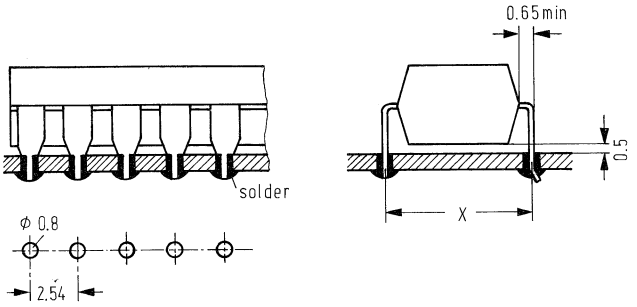
4. Incoming Inspection

Test procedures at the manufacturer's are intended to make incoming inspection unmecessary. If the buyer still requires inspection, it is recommended to use test procedures in accordance with AQL-table ABC-STD-105 D.

Mounting Instructions

Plastic dual-in-line package

Plastic packages are soldered on the side of the printed circuit board opposite to the case, the pins are vertically bent and fit into holes at an equal distance of 2.54 mm and a diameter of 0.7 to 0.9 mm. The distance X has to be taken from the corresponding package outline drawing.
The distance between the package and the printed circuit board is determined by shoulders (see picture).
After inserting the package into the printed circuit board two or more pins should be bent at an angle of app. 30 °C. Thus the package need not be held down while soldering.
The maximum allowable solder times are with iron soldering 265 °C (max. 10s) and with dip soldering 240 (max. 4s).



LSL-Series

FZ 100 is a low-speed noise-immune logic series of monolithic integrated circuits. A Zener-diode input as well as a relatively large collector capacitance of the input transistor ensure an excellent static and dynamic noise immunity of the integrated circuit. Propagation delay times can be adjusted with capacitors. Thust the dynamic noise immunity can be increased as required. Due to these advantages, the series FZ 100 is in particular suited for applications where strong noise endangers operations, and where the noise immunity is much more important than the switching speed.

1. Noise Immunity

1.1 Static Noise Immunity

The static noise immunity characterizes the behavior of a system disturbed by noise pulses which last longer than the average propagation delay time. The static noise immunity defines the voltage levels which do not influence the logic state. The typical values of the static noise immunity or noise margin are derived from the transfer function (figure 5). For the L-state follows:
at $V_S = 12$ V: $V_{nmL} = V_{T1} - V_{IL} = 5.9 - 0.9 = 5.0$ V
at $V_S = 15$ V: $V_{nmL} = V_{T2} - V_{IL} = 5.6 - 0.9 = 4.7$ V.

For the H-state follows:
at $V_S = 12$ V: $V_{nmH} = V_{QH} - V_{T1} = 11.3 - 5.9 = 5.4$ V
at $V_S = 15$ V: $V_{nmH} = V_{QH} - V_{T2} = 14.3 - 5.6 = 8.7$ V

The guaranteed noise immunity under worst-case conditions results as follows:
$V_{nmL} = V_{IL} - V_{QL} = 4.5 - 1.7 = 2.8$ V at $V_S = 12$ and 15 V
$V_{nmH} = V_{QH} - V_{IH} = 10 - 7.5 = 2.5$ V at $V_S = 12$ V and
$V_{nmH} = V_{QH} - V_{IH} = 12 - 7.5 = 4.5$ V at $V_S = 15$ V.

1.2 Dynamic Noise Immunity

The dynamic noise immunity characterizes the behavior of a system disturbed by noise pulses of a shorter duration than the signal propagation delay time. In this case the energy of the noise pulse – pulse amplitude and duration – determines whether a change of the logic state will take place.
The practical aspects of the dynamic noise immunity are the input noise immunity and the immunity against capacitively coupled noise. The source of capacitively coupled noise can either be cross talk (system noise) or foreign noise. A coupling capacitance of up to 1.6 nF typically does not introduce any cross talk. Due to this value, system noise can in general be regarded as being a minor problem, and foreign noise sources only have to be considered as important.
The following figures show the noise immunity of the complementary MOS-logic CMOS and the low-speed noise-immune logic LSL.

1.2.1 Input noise immunity

Pulse duration and amplitude of a noise pulse are limited by the propagation delay time t_P of a gate. The noise amplitude may become greater than the static noise immunity if the noise pulse duration $b \leqq \frac{1}{2} t_P$. The noise amplitude may not exceed the static noise immunity if $b \geqq t_P$. However, t_P can be adjusted as required by an integrating capacitance C.

Figures 1 and 2 show the typical input noise immunity of NAND-gates with and without integrating capacitance at supply voltages V_S = 12 V. The noise voltage V_{nm} is shown as a function of the noise pulse duration *b*. Figure 2 indicates the more critical case where an L-signal at the input is disturbed. This is due to the transition time t_{THL} being shorter than t_{TLH}. Thus the noise pulse duration at L-level is less than at H-level.

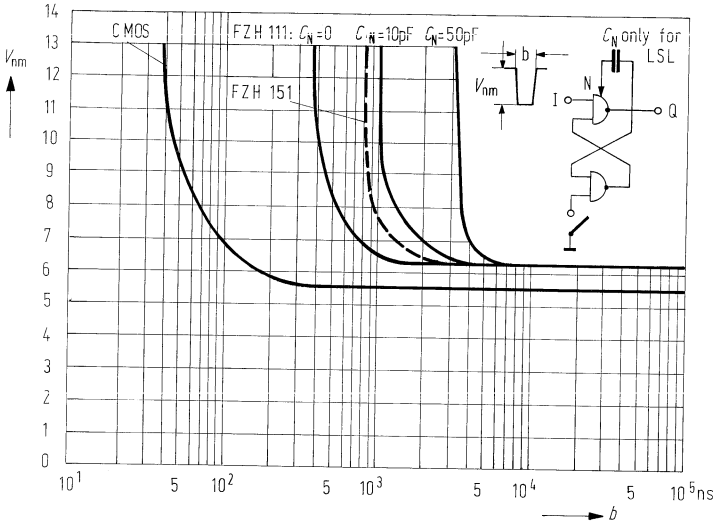


Fig. 1
Typical boundary characteristic for input noise at H-level
$V_{nm} = f(b)$ at $V_S = 12$ V

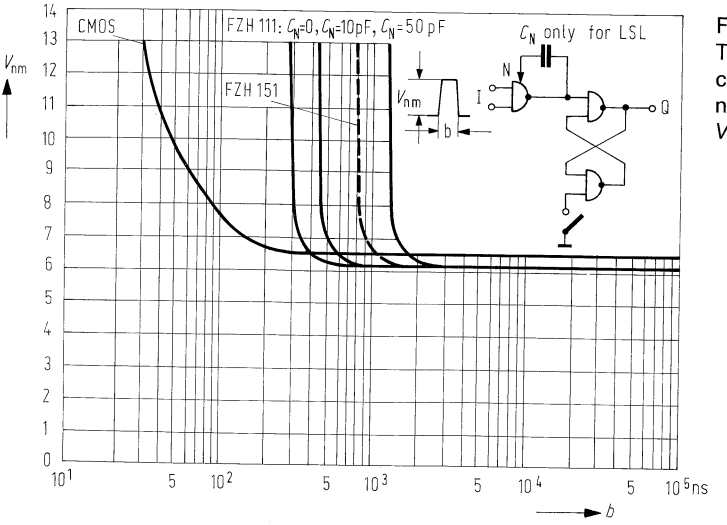


Fig. 2
Typical boundary characteristic for input noise at L-level
$V_{nm} = f(b)$ at $V_S = 12$ V

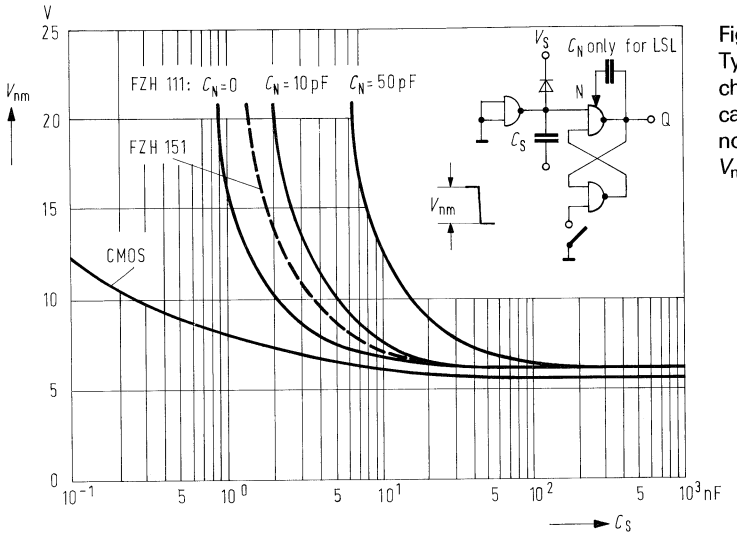


Fig. 3
Typical boundary characteristic for capacitively coupled noise at H-level
$V_{nm} = f(C_S)$ at V_S = 12 V

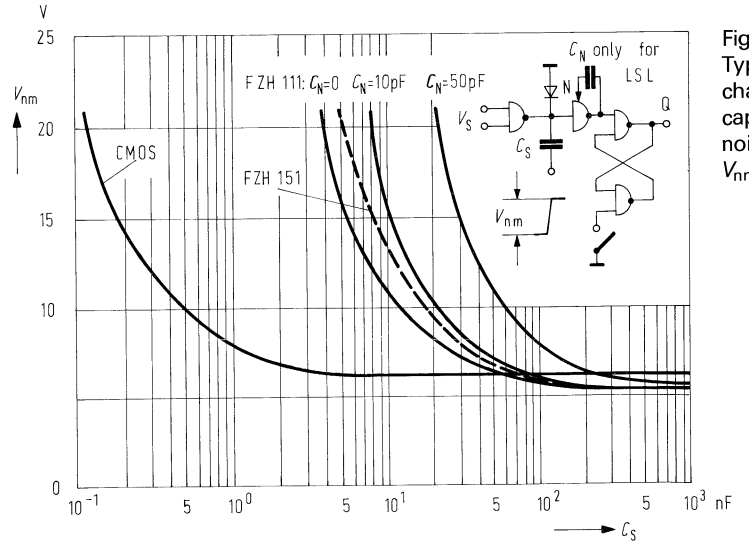


Fig. 4
Typical boundary characteristic for capacitively coupled noise at L-level
$V_{nm} = f(C_S)$ at V_S = 12 V

1.2.2

The push-pull output stage generally used with LSL-circuits has a low output resistance in both logic states ($R_{QL} \sim 20\ \Omega$ and $R_{QH} \sim 400\ \Omega$). The resulting time constants are relatively small, and noise pulses die away rapidly. Figures 3 and 4 show the typical noise immunity against capacitively coupled noise of NAND-gates with and without integrating capacitance at supply voltages $V_S = 12$ V. The noise voltage V_{nm} is shown as a function of the coupling capacitance C_S. The more critical case is given in Figure 3 where an H-state is disturbed. This is due to the H-output resistance being greater than the L-output resistance.
The transition time of the noise source was approximately 1 ns and the source resistance approximately 1Ω.

1.3. Destruction Energy

The amount of energy permissible at any terminal of an LSL-circuit without danger of destruction is typically 1 mWs per circuit. A suitable protective circuit is shown in paragraph 5.1.

2. Description of the Static Characteristics

2.1 Maximum Ratings

Maximum ratings are absolute limits. The integrated circuit may be destroyed if a single value is exceeded. Maximum ratings are valid at T_A = 25 °C unless noted otherwise.

2.2 Electrical Characteristics

Typical characteristics are statistic mean values. In most cases they are supplemented by guaranteed distribution boundaries. Typical characteristics are valid at T_A = 25 °C and recommended supply voltages V_S = 12 V and 15 V respectively.

2.3 Characteristic Functions

2.3.1 Transfer function

Figure 5 shows the typical transfer function $V_Q = f(V_I)$ of NAND-gates at supply voltages V_S = 12 V and 15 V. The transfer function is almost independent of the output load.
To ensure safe operation, the input voltage must surpass the threshold voltage V_T. The threshold voltage is determined graphically at the intersection of the transfer function with the straight line $V_I = V_Q$.

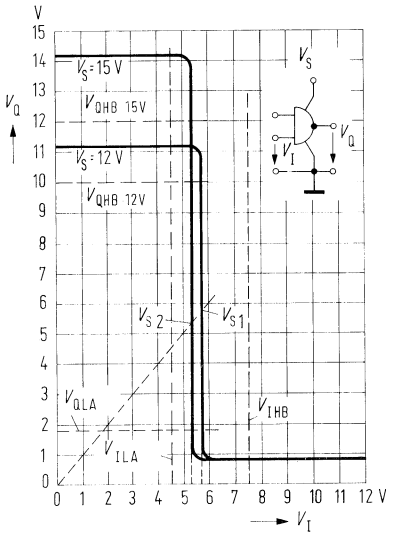


Fig. 5
Typical transfer function of NAND-gates $V_Q = f(V_I)$

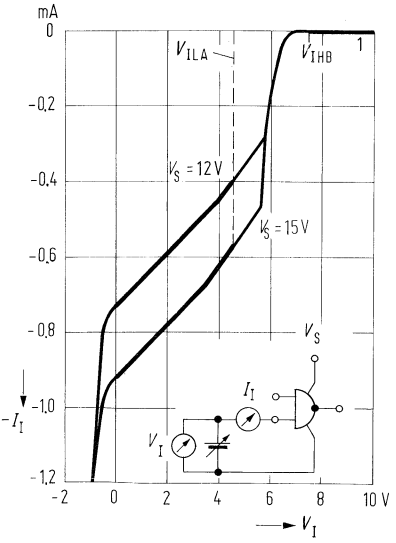


Fig. 6
Typical input characteristic $I_I = f(V_I)$

2.3.2 Input characteristic

Figure 6 shows the typical input characteristic $I_I = f(V_I)$ at supply voltages V_S = 12 and 15 V. The input characteristic can be divided into 3 ranges:

1. Only a small reverse current of approximately 1 μA flows into the input if the input is supplied with an H-level. The breakdown voltage of the diodes is typically 30 V and may not be exceeded.
2. If an L-level is applied to the input, the input current reverses its direction.
3. The substrate diodes start conducting at negative input voltages. The input current increases rapidly. Maximum negative ratings must be observed.

The input characteristic is independent of the load as the gate circuit does not include feedback. The TTL-LSL-level-converter FZH 181/185 has an input characteristic similar to TTL-circuits.

2.3.3 Output characteristics

Figure 7 shows the typical output characteristic of the L-state $V_{QL} = f(I_{QL})$ for normal outputs and power outputs at supply voltages V_S = 12 V and 15 V. The current I_{QL} is sunk by the gate output. The output characteristic indicates that the output current may exceed the rated load current stated in the data sheet for the output voltage V_{QL} = 1.7 V. The current limit is given by the total power dissipation per package of 500 mW which must not be exceeded.

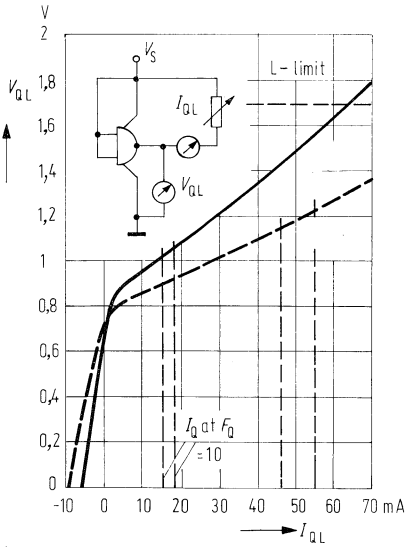


Fig. 7
Typical output characteristic of the L-state $V_{QL} = f(I_{QL})$ for normal outputs (——) and power outputs (- - -) at V_S = 12/15 V

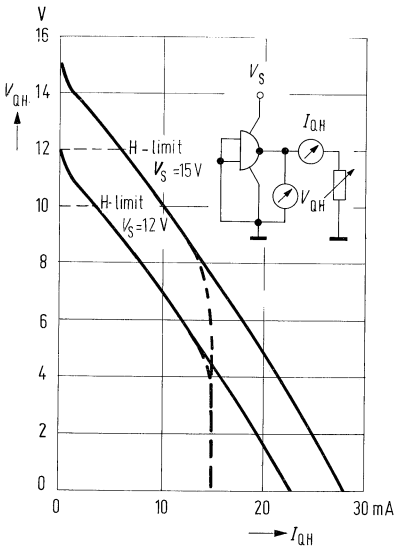


Fig. 8
Typical output characteristic of the H-state $V_{QH} = f(I_{QH})$,
—— FZH 101/5 through FZH 171/5, FZJ 101/5, and FZJ 111/115
- - - FZH 191/5 through FZH 291/5, FZJ 121/5 through FZJ 161/5, and FZK 101/5

Figure 8 shows the typical output characteristic of the H-state $V_{QH} = f(I_{QH})$ at supply voltages V_S = 12 V and 15 V. Here the output current I_Q is supplied by the gate output. Not more than one output may be shorted at the same time. The maximum short circuit duration is 1 µs for circuits without short circuit protection. The dotted part of the curve applies for circuits with short circuit current limiting. The circuits are thus protected from damage.

2.4 Logical data

2.4.1 Input load factor

The input load factor defines the currents required by a single input at H-state as well as L-state. The upper limit of the H-input current per input is I_{IHA} = 1 µA. The upper limit of the L-input current per input is I_{ILA} = −1.5 mA at V_S = 12 V and −1.8 mA at V_S = 15 V. These values define the normalized load factor F_I = 1. They are valid within the entire temperature range.
F_I = 2 means for example an L-input current of $-I_{IL}$ = 2 x 1.5 = 3 mA at V_S = 12 V and $-I_{IL}$ = 2 x 1.8 = 3.6 mA at V_S = 15 V and an H-input current of I_{IH} = 2 x 1 = 2 µA.

2.4.2 Output load factor

The output load factor defines how many normalized loads F_I=1 can be driven by a single output The H-output load factor is higher than the L-output load factor. In this way it is possible to connect unused inputs of the same gate in parallel without accounting for an additional load.

3. Description of the Dynamic Characteristics

3.1 **Load capacitance**

Figure 9 shows the influence of capacitive loading on the switching parameters. It can be seen that rather large values are necessary to decrease the speed. Thus long connection lines may be easily used.

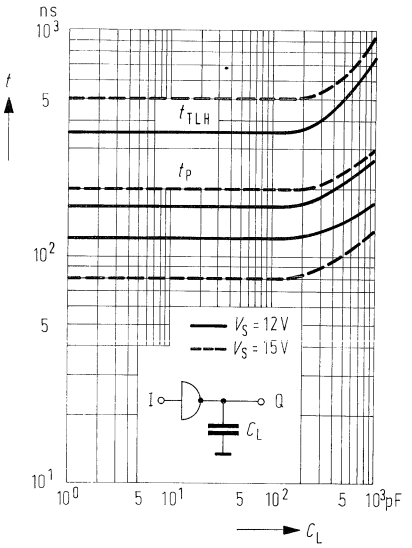


Fig. 9
Typical switching parameters as a function of the load capacitance $t = f(C_L)$,
t_T = transition time, t_P = propagation delay.

3.2 **Delay capacitance**

Due to a special geometry of the input transistor the collector capacitance is relatively great. This causes long propagation delay times and a high dynamic noise immunity results. Circuits with an N-node enable the designer to lengthen the propagation delay times with an integrating capacitor C_N Thus the dynamic noise immunity can be adapted as required. The capacitor is connected between output Q and N-node with gates. Flipflops require two capacitors to delay the slave. One between output Q and node N_Q and another one between output $\bar{Q}$ and node $N_{\bar{Q}}$. Two additional capacitors may be provided at the nodes N_J, N_J and N_K, N_K of the flipflops FZJ 111/115 to increase the noise immunity of the master. No limit is given for the integrating capacitance for gates and flipflops.

C_N must be connected between the N-input and ground O_S with the circuits FZK 101/105, FZJ 141/145, FZJ 151/155 and FZJ 161/165. The upper limit of C_N is 500 pF for the FZK 101/105 and 1 nF for the remaining circuits.

Figure 10 shows the switching parameters as a function of the capacitance C_N for gates at supply voltages V_S = 12 V and 15 V.

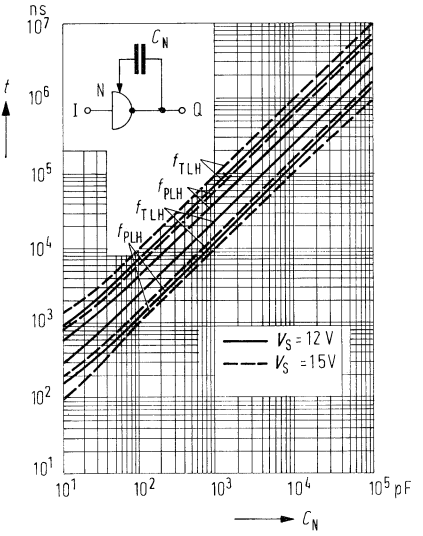


Fig. 10
Typical switching parameters of gates as a function of the integrating capacitance $t = f(C_N)$.
t_T = transition time,
t_P = propagation delay

Figures 11 and 12 show the typical switching parameters for flipflops between clock input C and Q as well as the reset input $\overline{R}$ and Q as a function of the integrating capacitance C_N at supply voltages V_S = 12 V and 15 V.

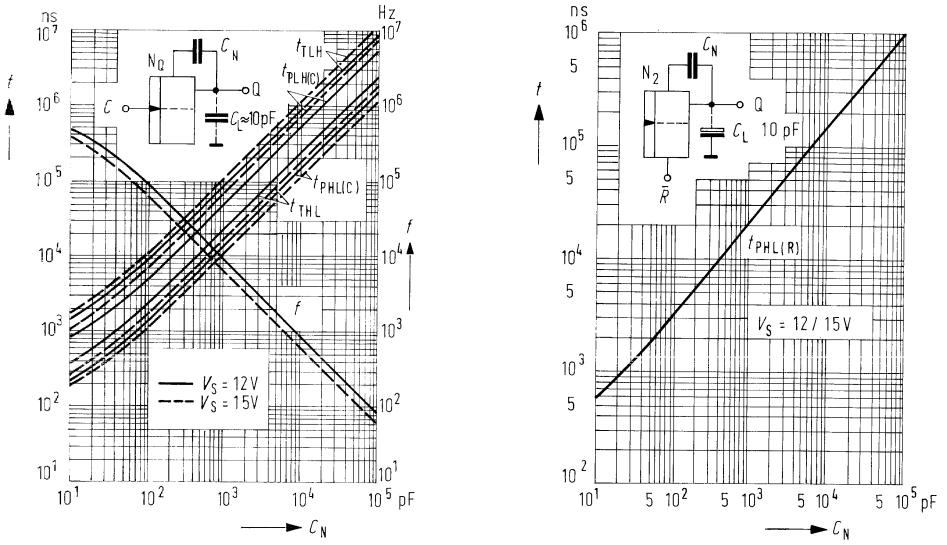


Fig. 11 and 12
Typical switching parameters of flipflops as a function of the integrating capacitance $t = f(C_N)$.
t_T = transition time, t_P = propagation delay

The characteristics are referred to the Q-output only. Identical results will be achieved for measurements between C and output $\overline{Q}$ and the set input $\overline{S}$ and $\overline{Q}$. The maximum clock frequency f can directly be derived from the switching parameters as shown in fig. 11. The integrating capacitance also determines the dutycycle of the clock pulse. While the clock pulse duration $t_{pH(C)}$ depends on the capacitance at the master, the clock pause $t_{pL(C)}$ is defined by the capacitance at the slave. The corresponding diagram is shown in figure 13. The actual dutycycle is given by the formula:

$t_p = t_{pL(C)} + t_{pH(C)}$

As no integrating capacitance is provided at the master of the FZJ 101/105, the minimal value of the clock pulse duration has to be inserted.

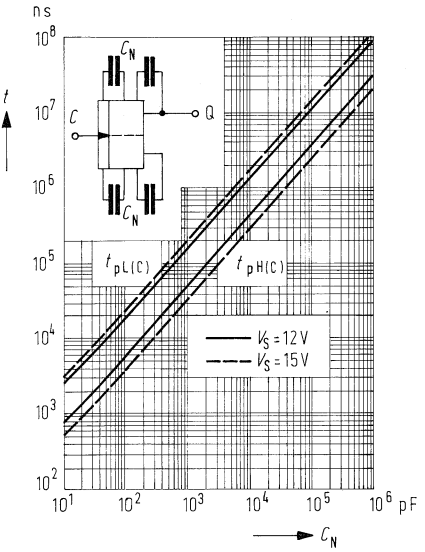


Fig. 13
Typical dutycycle of the clock pulse as a function of the integrating capacitance $t_p = f(C_N)$

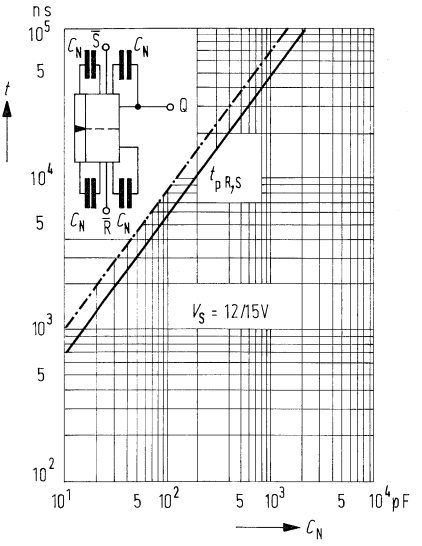


Fig. 14
Typical (——) and minimal (– · –) set and reset pulse duration as a function of the integrating capacitance $t_p = f(C_N)$

Figure 14 shows the required increase of the set and reset pulse duration as a function of the integrating capacitance C_N at supply voltages V_S = 12 V and 15 V. No integrating capacitance is provided at the master of the FZJ 101/105. Thus the diagram applies only at C = H, when master and slave are disconnected.

3.3 **Propagation Delay and Transition Time**

The propagation delay time t_{PLH} is measured between input and output while the output rises from L to H-level. Whereas t_{PHL} is determined when the output switches from H to L. Reference points for the propagation delay time are the levels 4.5 V.
The transition times t_{THL} and t_{THL} of the output pulse are measured between the 10% and 90% values.
The pair-delay defines the signal delay which is caused by two NAND-gates connected in series. The output signal is then in phase with the input signal, however delayed by:
$t_{PD} = t_{PHL} - t_{PLH}$
Figure 9 shows that the switching parameters are nearly independent of the load capacitance. This is due to a low output resistance at the L-state as well as the H-state. In this way it is possible to use long connection lines which represent essentially a capacitive load. The switching parameters remain constant over a wide range.
Figures 15 through 19 show the signal propagation delay times as well as the transition time as a function of the supply voltage V_S over the entire operating range of 11.4 to 17 V.

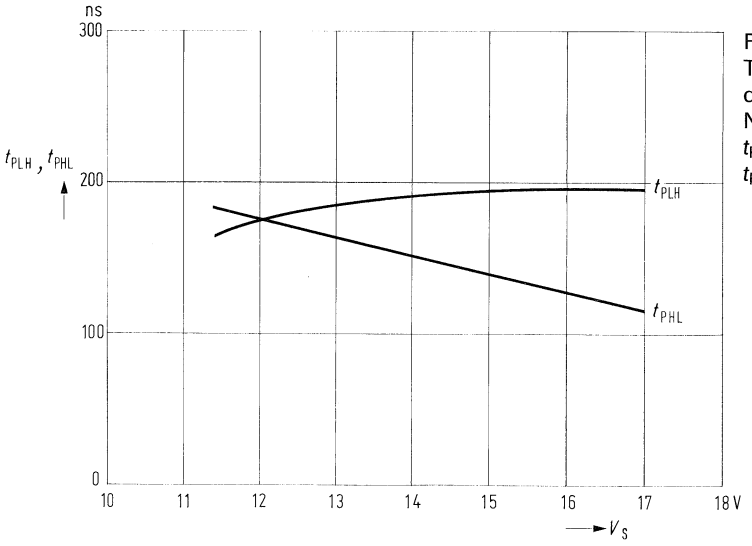


Fig. 15
Typical propagation delay times of NAND-gates
$t_{PLH} = f(V_S)$
$t_{PHL} = f(V_S)$

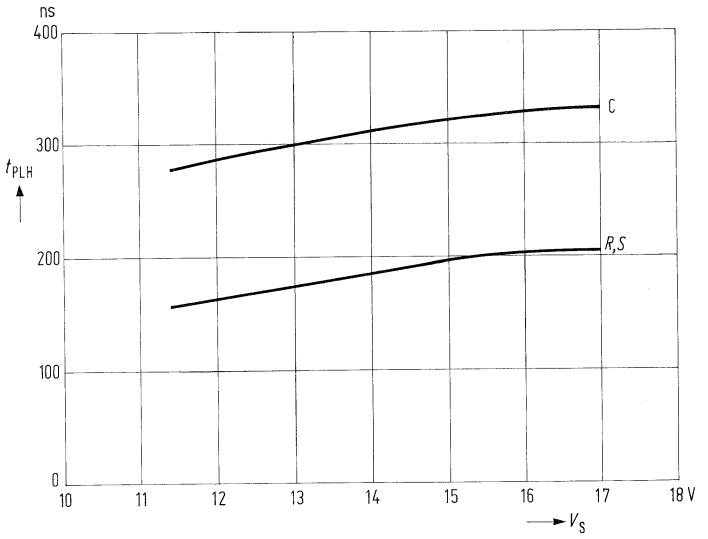


Fig. 16
Typical propagation delay times of flipflops
$t_{PLH} = f(V_S)$
C = clock input
R, S = reset and set inputs

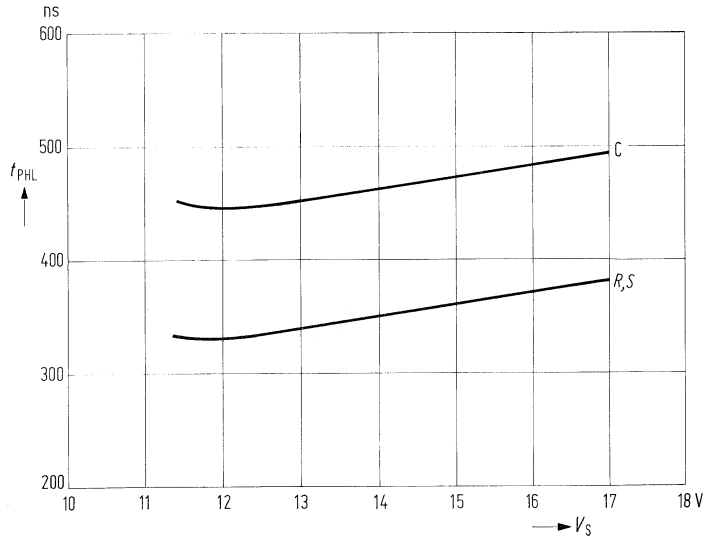


Fig. 17
Typical propagation delay times of flipflops
$t_{PHL} = f(V_S)$
C = clock input
R, S = reset and set inputs

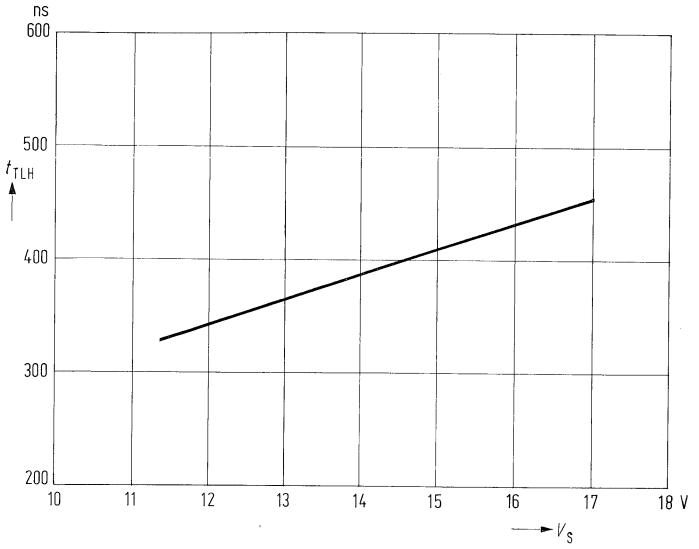


Fig. 18
Typical transition time of NAND-gates and flopflops
$t_{TLH} = f(V_S)$

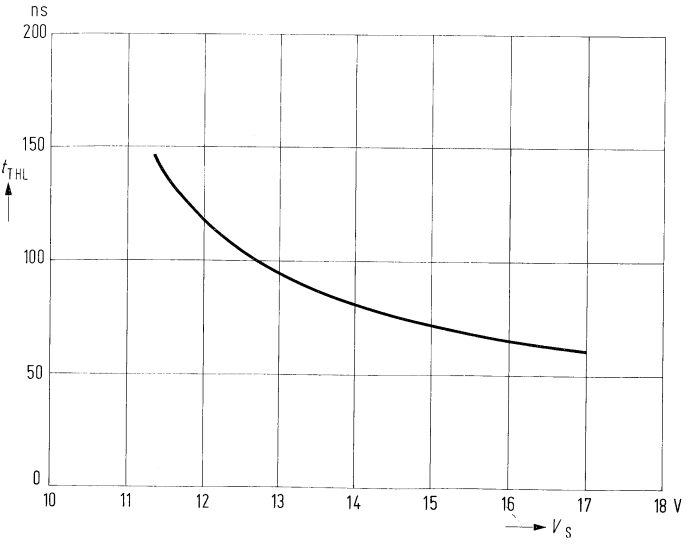


Fig. 19
Typical transition time of NAND-gates and flipflops
$t_{THL} = f(V_S)$

Electrical Characteristics

4. Electrical Characteristics

General Information on the LSL-Series FZ 100

The electrical characteristics are given for two supply voltage ranges. The limits of the 12 V-range are V_{SB} = 11.4 V and V_{SA} = 13.5 V. The limits of the 15 V-range are V_{SB} = 13.5 V and V_{SA} = 17.0 V. Typical values are valid at the corresponding nominal voltages and an ambient temperature T_A = 25 °C.

Maximum Ratings

		lower limit B	upper limit A	unit
Supply voltage except FZH 181/185	V_S	0	18	V
Supply voltage FZH 181/185	V_S	0	7	V
Input voltage except FZH 181/185	V_I	0	18	V
Input voltage FZH 181/185	V_I	0	5.5	V
Voltage at the node N	V_N	−1	0.6	V
Current at the node N	I_N	−10	2	mA
Ambient temperature range 1	T_A	0	70	°C
range 5	T_A	−25	85	°C
Storage temperature	T_S	−65	150	°C

Maximum Negative Ratings at T_A = 0 to 70 °C

	V_I V	I_I mA	at V_S V
Any input except N-nodes of any circuit except:			
FZH 151/155, FZH 181/185 and expander inputs of FZH 171/175		−25	17
FZH 151/155	−0.7		17
FZH 181/185	−0.5	−25	5

Application note

Pins shown unconnected in the pin configuration must be left open.
Transition times for circuits without delay capacitance should be below 1 V/µs.
When changing from delayed circuits to undelayed circuits the transition time has to be increased sufficiently.

FZH 101/105 Quadruple 2-Input NAND-Gate
FZH 111/115 Quadruple 2-Input NAND-Gate with N-Input
FZH 101A/105A and FZH 111A/115A will shortly be available with short-circuit-proof output as shown in fig. 8
FZH 121/125 Dual 5-Input NAND-Gate
FZH 131/135 Dual 5-Input NAND-Gate with N-Input
FZH 171/175 Dual 4-Input NAND-Gate with Expander Nodes N_1 and N-Input

Electrical Characteristics

12 V-range temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SA}$ and V_{SB}	2			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} $V_{IL}=4.5$ V $-I_{QH}=0.1$ mA	2	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V $I_{QL}=15$ mA	1		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input except N	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	3			1.0	µA
L-input current, each input except N	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	4		0.8	1.5	m
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ $V_I=V_Q=0$ V	5	10	30	50	m
H-supply current, each gate	I_{SH}	$V_S=V_{SA}$ $V_I=0$ V	6		0.9	1.6	m
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$	7		1.7	3.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1:1			16	31	mW

Delay times, $V_S=12$ V, $F_Q=1$, $T_A=25$ °C

Propagation delay	t_{PLH}	$C_L=10$ pF at 4.5V above ground	26	90	175	310	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}	$C_L=10$ pF		200	340	570	ns
	t_{THL}			70	120	210	ns

Electrical Characteristics

15 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}	2			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA} $V_{IL} = 4.5$ V $-I_{QH} = 0.1$ mA	2	12.0	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$ $V_{IH} = 7.5$ V $I_{QL} = 15$ mA	1		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input except N	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	3			1.0	μA
L-input current, each input except N	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	4		1.0	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$ $V_I = V_Q = 0$ V	5	15	37	60	mA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$ $V_I = 0$ V	6		1.2	2.1	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$ $V_I = V_{IHA}$	7		2.3	4.0	mA
Power consumption, each gate	P	$V_S = V_{SA}$ duty cycle 1:1			27	52	mW

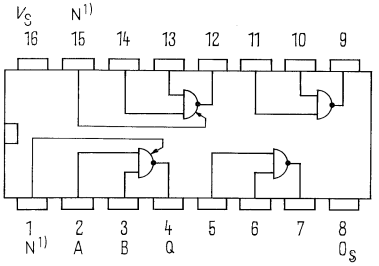
Delay times, $V_S = 15$ V, $F_Q = 1$, $T_A = 25$ °C

Propagation delay	t_{PLH}	$C_L = 10$ pF at 4.5V above ground	26		195		ns
	t_{PHL}				140		ns
Transition time	t_{TLH}	$C_L = 10$ pF			410		ns
	t_{THL}				75		ns

Quadruple 2-Input NAND-Gate

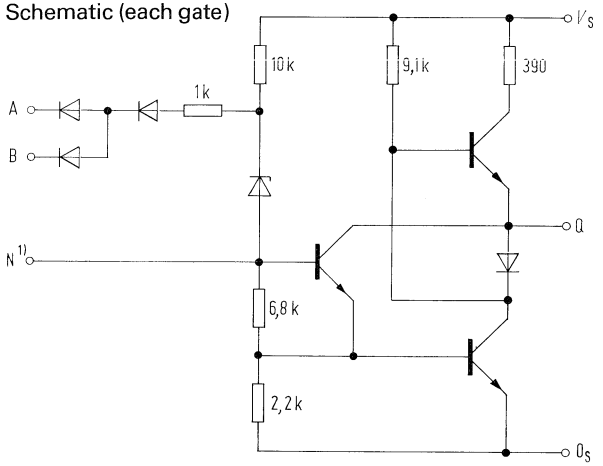
FZH 101
FZH 105
FZH 111
FZH 115

Type	order numbers
FZH 101	Q 67000–H 190
FZH 105	Q 67000–H 250
FZH 111	Q 67000–H 191
FZH 115	Q 67000–H 215



Pin configuration
top view

Schematic (each gate)



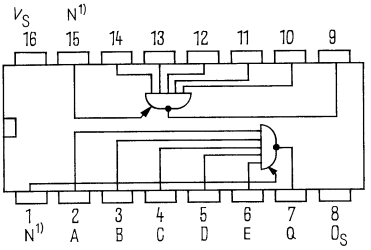
Logical data, each gate			upper limit A
Output load factor	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1
Logic		$Q = \overline{AB}$	

1) Gates 1 and 4 of FZH 111/115 only

Dual 5-Input NAND-Gate

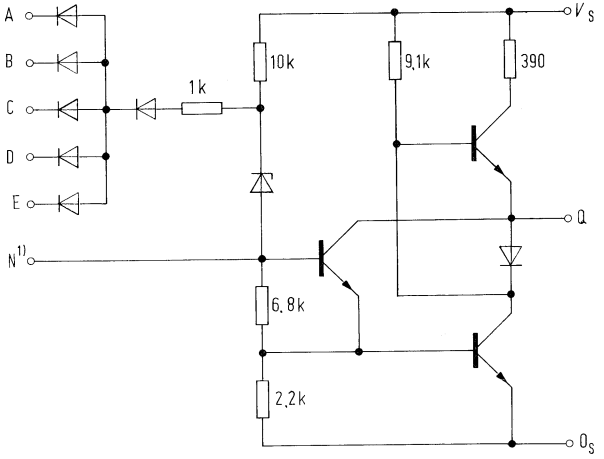
FZH 121
FZH 125
FZH 131
FZH 135

Type	order numbers
FZH 121	Q 67000–H 192
FZH 125	Q 67000–H 254
FZH 131	Q 67000–H 193
FZH 135	Q 67000–H 255



Pin configuration
top view

Schematic (each gate)



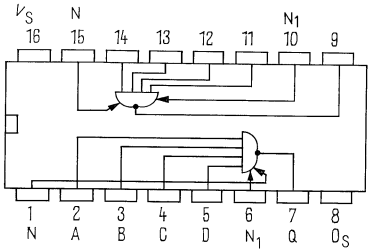
Logical data, each gate			upper limit A
Output load factor	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1

Logic $Q = \overline{ABCDE}$

1) FZH 131/135 only

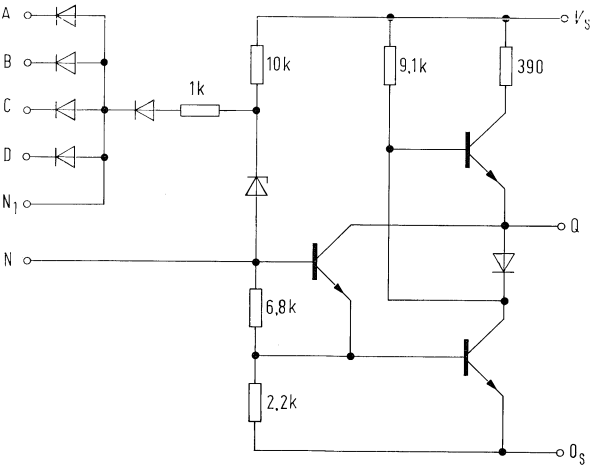
Type	order numbers
FZH 171	Q 67000–H 328
FZH 175	Q 67000–H 329

The number of inputs can be expanded as required by means of additional input diodes BAW 76 at the expander input N_1. The anodes of the diodes must be connected in parallel to N_1.



Pin configuration
top view

Schematic (each gate)



Logical data, each gate			upper limit A
Output load factor	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1

Logic $Q = \overline{ABCDN_1}$

Type	order numbers
FZH 141	Q 67000-H 194
FZH 145	Q 67000-H 256

The electrical characteristics of the FZH 141/145 are similar to the FZH 131/135 except for the values stated below.

Electrical characteristics
12 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
L-output voltage	V_{QL}	$V_S = V_{SB}$ V_{IH} = 7.5 V I_{QL} = 45 mA	1		1.3	1.7	V

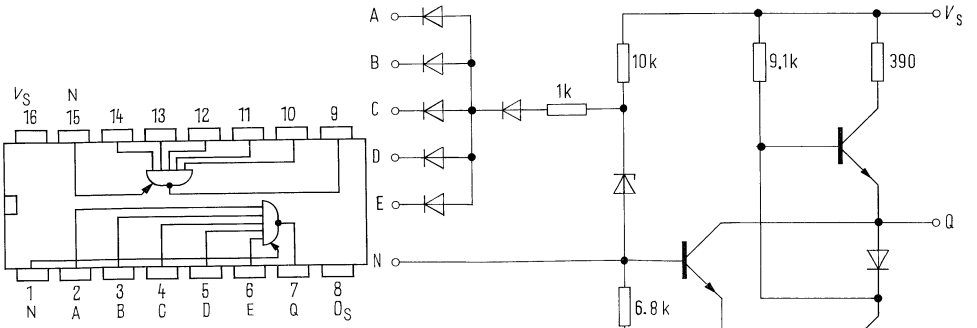
Electrical characteristics
15 V-range
temperature ranges 1 and 5

L-output voltage	V_{QL}	$V_S = V_{SB}$ V_{IH} = 7.5 V I_{QL} = 54 mA	1		1.4	1.7	V

Logical data, each gate

Output load factor H-signal	F_{OH}					100	
L-signal	F_{OL}					30	
Input load factor, each input	F_I					1	

Logic $Q = \overline{ABCDE}$



Pin configuration
top view

Schematic (each gate)

Type	order numbers
FZH 151	Q 67000–H 195
FZH 155	Q 67000–H 260

The FZH 151/155 are suited for the following applications:
AND/OR-gate, flipflop, counter, divider, shiftregister, adder, delay element. The lower limit of the supply voltage is V_S=10 V.

Electrical characteristics

12 V-range temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	15	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$	16			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ V_{IL}=4.5 V $-I_{QH}$=0.1 mA	16	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ V_{IH}=7.5 V I_{QL}=30 mA	15		0.9	1.7	V
DC noise margin							
H-signal	V_{SS}			2.5	5.0		V
L-signal	V_{SS}			2.8	5.0		V
H-input current at R_1, C_1, R_2, C_2	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	17			2.0	µA
H-input current remaining inputs except N	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	17			1.0	µA
L-input current at R_1, C_1, R_2, C_2	$-I_{IL}$	$V_S=V_{SA}$ V_{IL}=1.7 V	18		1.0	2.5	mA
L-input current remaining inputs except N	$-I_{IL}$	$V_S=V_{SA}$ V_{IL}=1.7 V	18		0.5	1.25	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ $V_I=V_Q$=0 V	19	10	30	50	mA
H-supply current	I_{SH}	$V_S=V_{SA}$ V_I=0 V	20		14.0	22.0	mA
L-supply current	I_{SL}	$V_S=V_{SA}$ $V_I=V_{SA}$	21		8.0	15.0	mA
Power consumption	P	$V_S=V_{SA}$ duty cycle 1 :1			132	250	mW

Delay times, V_S=12 V, F_Q=1, T_A=25 °C

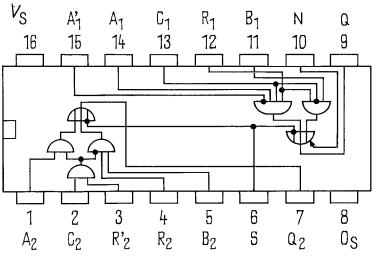
		test condition		test cct.	lower limit B	typ.	upper limit A	unit
Propagation delay	t_{PLHI}	output signal non-inverted	C_L= 10 pF	27		340		ns
	t_{PLHII}	output signal inverted				340		ns
	t_{PLHIII}	input pin 15				270		ns
Propagation delay	t_{PHLI}	output signal non-inverted				230		ns
	t_{PHLII}	output signal inverted				300		ns
	t_{PHLIII}	input pin 15				400		ns
Transition time	t_{TLH}	C_L=10 pF				330		ns
	t_{THL}					200		ns

Electrical characteristics

15 V-range temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	15	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$	16			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ $V_{IL}=4.5$ V $-I_{QH}=0.1$ mA	16	12.0	14.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V $I_{QL}=30$ mA	15		1.0	1.7	V
DC noise margin							
H-signal	V_{SS}			4.5	8.0		V
L-signal	V_{SS}			2.8	5.0		V
H-input current at R_1, C_1, R_2, C_2	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	17			2.0	µA
H-input current remaining inputs except N	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	17			1.0	µA
L-input current at R_1, C_1, R_2, C_2	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	18		1.2	3.0	mA
L-input current remaining inputs except N	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	18		0.6	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ $V_I=V_Q=0$ V	19	15	37	60	mA
H-supply current	I_S	$V_S=V_{SA}$ $V_I=0$ V	20		18.0	29.0	mA
L-supply current	I_{SL}	$V_S=V_{SA}$ $V_I=V_{SA}$	21		12.0	21.0	mA
Power consumption	P	$V_S=V_{SA}$ duty cycle 1 : 1			225	425	mW

Delay times, $V_S=15$ V, $F_Q=1$, $T_A=25$ °C

Propagation delay	t_{PLHI}	output signal non-inverted	$C_L=$ 10 pF	27			ns
	t_{PLHII}	output signal inverted					ns
	t_{PLHIII}	input pin 15					ns
Propagation delay	t_{PHLI}	output signal non-inverted					ns
	t_{PHLII}	output signal inverted					ns
	t_{PHLIII}	input pin 15					ns
Transition time	t_{TLH}	$C_L=10$ pF					ns
	t_{THL}						ns



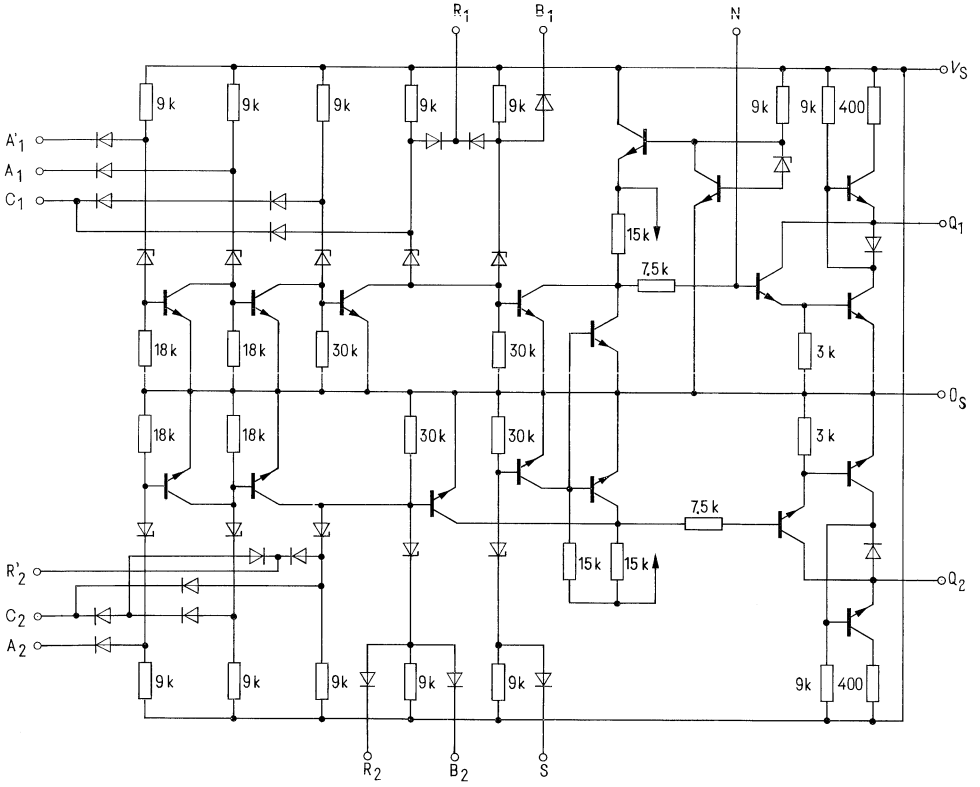
Pin configuration
top view

Logical data, each gate		upper limit A
Output load factor		
H-signal	F_{OH}	100
L-signal (LSL load)	F_{OL}	16
L-signal (FZH 151 as load)	F_{OL}	20
Input load factor at R_1, C_1, R_2, C_2	F_I	2
Input load factor, remaining inputs	F_I	1

Logic

$$Q_1 = \overline{S} + (A_1\overline{A}'_1R_1C_1) + (B_1R_1\overline{C}_1)$$
$$Q_2 = \overline{S} + (A_2C_2R'_2) + (B_2R_2\overline{C}_2\overline{R}'_2)$$

Schematic


R1
B1
N
VS
A'1
A1
C1
9k
400
15k
7,5k
Q1
18k
30k
3k
QS
R'2
C2
A2
15k
Q2
R2
B2
S

Type	order numbers
FZH 161	Q 67000–H 288
FZH 165	Q 67000–H 289

The FZH 161/165 may also be used as LSL-wired-AND stages. The collector load resistance is calculated according to the formulaes stated on the following pages. The upper limit of the breakdown voltage at the Q-outputs is 18 V.

Electrical characteristics

12 V-range temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	9	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$	10			4.5	V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V $I_{QL}=20$ mA	9			0.4	V
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current except N							
at input pins 2, 5, 11, 14	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$	11			1.0	µA
at input pins 1, 15	I_{IH}					2.0	µA
L-input current except N							
at input pins 2, 5, 11, 14	$-I_{IL}$	$V_S=V_{SA}$, $V_{IL}=1.7$V	12		0.8	1.5	mA
at input pins 1, 15	$-I_{IL}$				1.6	3.0	mA
H-output current, each output	I_{QH}	$V_S=V_{SA}$, $V_Q=18$ V	10			80	µA
H-supply current, each gate	I_{SH}	$V_S=V_{SA}$, $V_I=0$ V	14		2.5	4.5	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$, $V_I=V_{IHA}$	13		4.0	6.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1 : 1			39	70	mW

Delay times, $V_S=12$ V, $T_A=25$ °C

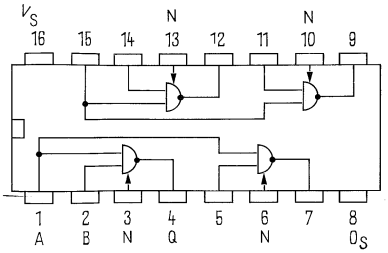
Propagation delay	t_{PLH}	$C_L=15$ pF, $R_C=760$, $V_{SC}=12$V	28	80	250	500	ns
	t_{PHL}			80	130	300	ns
	t_{PLH}	$C_L=15$ pF, $R_C=320$, $V_{SC}=5$V	28	80	230	500	ns
	t_{PHL}			80	120	300	ns
Transition times	t_{TLH}	$C_L=15$ pF, $R_L=760$, $V_{SC}=12$V	28	50	75	100	ns
	t_{THL}			15	30	50	ns
	t_{TLH}	$C_L=15$ pF, $R_C=320$, $V_{SC}=5$V	28	20	45	70	ns
	t_{THL}			6	12	25	ns

Electrical characteristics

15 V-range temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15	17.0	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	9	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$	10			4.5	V
L-output voltage	V_{QL}	$V_S = V_{SB}$ $V_{IH} = 7.5$ V $I_{QL} = 20$ mA	9			0.4	V
DC noise margin							
H-signal	V_{nm}			4.5	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current except N							
at input pins 2, 5, 11, 14	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	11			1.0	µA
at input pins 1, 15	I_{IH}					2.0	µA
L-input current except N							
at input pins 2, 5, 11, 14	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$V	12		1.0	1.8	mA
at input pins 1, 15	$-I_{IL}$				2.0	3.6	mA
H-output current, each output	I_{QH}	$V_S = V_{SA}$, $V_Q = 18$ V	10			80	µA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$, $V_I = 0$ V	14		2.8	4.5	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	13		4.5	7.0	mA
Power consumption, each gate	P	$V_S = V_{SA}$ duty cycle 1 : 1			55	78	mW

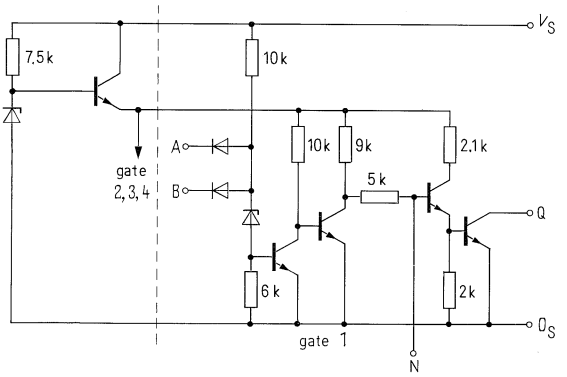
Delay times, $V_S = 15$ V, $T_A = 25$ °C

Propagation delay	t_{PLH}	$C_L = 15$ pF, $R_C = 760$, $V_{SC} = 12$V	28				ns
	t_{PHL}						ns
	t_{PLH}	$C_L = 15$ pF, $R_C = 320$, $V_{SC} = 5$V	28				ns
	t_{PHL}						ns
Transition times	t_{TLH}	$C_L = 15$ pF, $R_L = 760$, $V_{SC} = 12$V	28				ns
	t_{THL}						ns
	t_{TLH}	$C_L = 15$ pF, $R_C = 320$, $V_{SC} = 5$V	28				ns
	t_{THL}						ns



Pin configuration
top view

Schematic (each gate)



Logical data, each gate		upper limit A
L-Output load factor	F_{OL}	10
Input load factor, input A	F_I	2
Input load factor, input B	F_I	1
Logic	$Q = \overline{AB}$	

Calculation of the Collector Load Resistance R_C

The collector load resistance is derived from the required output voltage and the input and output currents of the gates as follows:

$$R_{CA} = \frac{V_{SC} - V_{OH}}{nI_{QH} + NI_{IH}} \frac{V}{\mu A} \qquad R_{CB} = \frac{V_{SC} - V_{QL}}{I_{QL} - NI_{IL}} \frac{V}{\mu A}$$

where: V_{SC} = supply voltage of the load resistor
n = number of AND-connections
N = number of inputs connected.

The actual resistance used in the circuit must have a value between the limits A and B.

Applications as level-converters:

FZH 161/165, LSL-TTL: $R_{CA} = \frac{5 - 2.4}{n\,80 + N\,40} \frac{V}{\mu A}$ $R_{CB} = \frac{5 - 0.4}{20 - N\,1.6} \frac{V}{mA}$

where: $n_A = 2$ for $N_A = 10$

FZH 181/185, TTL-LSL$_{12V}$: R_{CA} $\frac{12 - 10}{n\,250 + N\,1} \frac{V}{\mu A}$ $R_{CB} = \frac{12 - 1.0}{50 - N\,1.5} \frac{V}{mA}$

TTL-LSL$_{15V}$: $R_{CA} = \frac{15 - 12}{n\,250 + N\,1} \frac{V}{\mu A}$ $R_{CB} = \frac{15 - 1.0}{50 - N\,1.8} \frac{V}{mA}$

where: $n_A = 4$ for $N_A = 25$

Applications with wired-AND-connections of the FZH 161/165:

12 V-range: R_{CA} $\frac{12 - 10}{n\,80 + N\,1} \frac{V}{\mu A}$ $R_{CB} = \frac{12 - 0.4}{20 - N\,1.5} \frac{V}{mA}$

15 V-range: R_{CA} $\frac{15 - 12}{n\,80 + N\,1} \frac{V}{\mu A}$ R_{CB} $\frac{12 - 0.4}{20 - N\,1.8} \frac{V}{mA}$

where: $n_A = 9$ for $N_A = 10$.

Applications with TTL-wired-AND-connections of the FZH 181/185: see formulae and resistance table of corresponding TTL-gate, e. g. FLH 201.

Type	order numbers
FZH 181	Q 67000-H 326
FZH 185	Q 67000-H 327

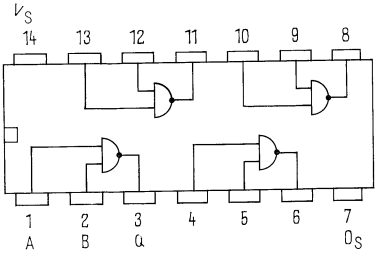
The FZH 181/185 may also be used as LSL-wired-AND stages. The collector load resistance is calculated according to the formulaes stated on the preceding page. The upper limit of the breakdown voltage at the Q-outputs is 18 V.

Electrical characteristics
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	tpy.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	1	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	8			0.8	V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2.0 V I_{QL}=16 mA	1			0.4	V
	V_{QL}	V_S=4.75 V V_{IH}=2.0 V I_{QL}=50 mA	1			1.0	V
DC noise margin	V_{nm}			0.4	1.0		V
Input current, each input	I_I	V_S=5.25 V V_I=5.5 V	3			1.0	mA
H-input current, each input	I_{IH}	V_S=5.25 V V_{IH}=2.4 V	3			80	µA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V	4			1.6	mA
H-output current, each output	I_{QH}	V_S=4.75 V V_{IL}= 0.8 V V_{QH}=18 V	8			250	µA
H-supply current, each gate	I_{SH}	V_S=5 V, V_I=0 V	6		1.0	2.0	mA
L-supply current, each gate	I_{SL}	V_S=5 V, V_I=5 V	7		8.5	12	mA
Power consumption, each gate	P	V_S=V_{SA} duty cycle 1:1			24	37	mW

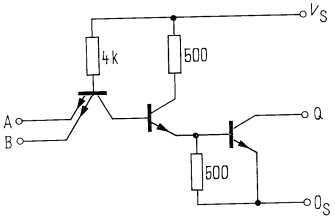
Delay times, V_S=5 V, T_A=25°C

Propagation delay	t_{PLH} t_{PHL}	C_L=15pF, R_C=760Ω	V_{SC}= 12 V	29		130 20	300 60	ns ns



Pin configuration
top view

Schematic (each gate)



Logical data, each gate		upper limit A
L-Output load factor	F_{OL}	10
Input load factor, each input	F_I	1
Logic	$Q = \overline{AB}$	

FZH 191/195 Triple 3-Input NAND-Gate with N-Input
FZH 201/205 Hex Inverter with Strobe Inputs

Electrical characteristics

12 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage				11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}	2			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} $V_{IL}=4.5$ V, $-I_{QH}=0.1$ mA	2	10.0	11.3		V
output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$V, $I_{QL}=15$mA	1		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current							
at strobe 1	I_{IH}					4.0	µA
at strobe 2	I_{IH}	$V_S=V_{SA}$	3			2.0	µA
remaining inputs except N	I_{IH}	$V_I=V_{IHA}$				1.0	µA
L-input current, each input except N	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	4		0.8	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$, $V_I=V_Q=0$ V	5	9	15	25	mA
H-supply current, each gate	I_{SH}	$V_S=V_{SA}$ $V_I=0$ V	6		0.9	1.6	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$	7		1.7	3.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1:1			15	31	mW

Delay times, $V_S=12$ V, $F_Q=1$, $T_A=25$ °C

Propagation delay	t_{PHL}	$C_L=10$ pF at 4.5 V above ground	26	90	175	310	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}	$C_L=10$ pF		200	340	570	ns
	t_{THL}			70	120	210	ns

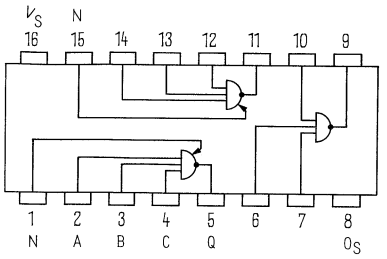
Electrical characteristics
15 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}	2			4.5	V
H-output voltage	V_{IH}	$V_S=V_{SB}$ and V_{SA} $V_{IL}=4.5$ V, $-I_{QH}=0.1$ mA	2	12.0	14.3		V
L-output voltage	V_{IL}	$V_S=V_{SB}$ $V_{IH}=7.5$V, $I_{QL}=18$mA	1		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current							
at strobe 1	I_{IH}	$V_S=V_{SA}$				4.0	μA
at strobe 2	I_{IH}	$V_I=V_{IHA}$	3			2.0	μA
remaining inputs except N	I_{IH}					1.0	μA
L-input current each input except N	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	4		1.0	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ $V_I=V_O=0$ V	5	9	15	25	mA
H-Supply current, each gate	I_{SH}	$V_S=V_{SA}$ $V_I=0$ V	6		1.2	2.1	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$	7		2.3	4.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1:1			27	46	mW

Delay times, $V_S=15$ V, $F_O=1$, $T_A=25$ °C

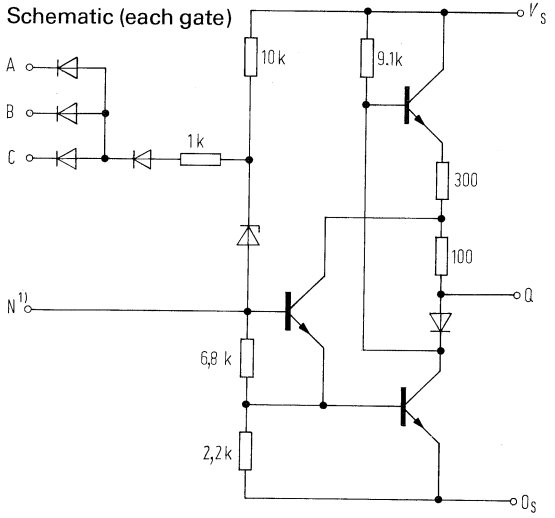
Propagation delay	410	t_{PLH}	$C_L=10$ pF at 4.5 V above ground	26	410		ns
		t_{PHL}			75		ns
Propagation delay		t_{TLH}	$C_L=10$ pF		95		ns
		t_{THL}			140		ns

Type	order numbers
FZH 191	Q 67000–H 633
FZH 195	Q 67000–H 634
FZH 201	Q 67000–H 636
FZH 205	Q 67000–H 637



Pin configuration
top view

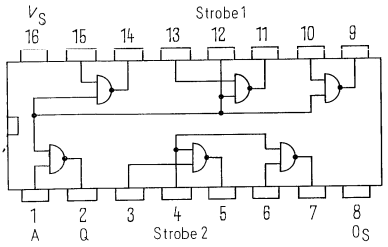
Schematic (each gate)



Logical date, each gate			upper limit A
Output load factor	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1
Logic		$Q = \overline{ABC}$	

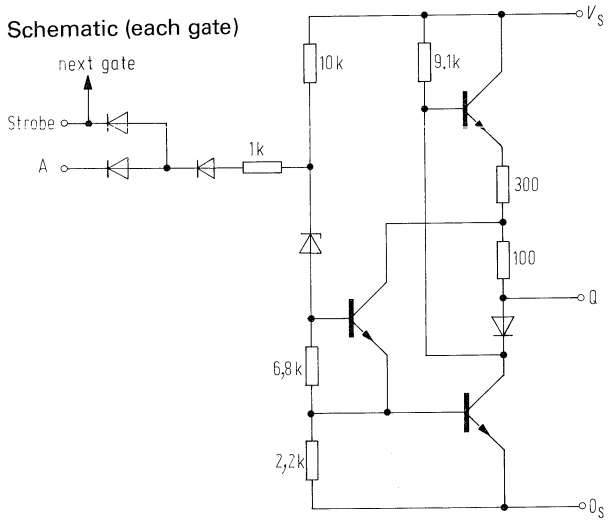
1) gates 1 and 3 only

Type	order numbers
FZH 191	Q 67000-H 633
FZH 195	Q 67000-H 634
FZH 201	Q 67000-H 636
FZH 205	Q 67000-H 637



Pin configuration
top view

Schematic (each gate)



Logical data, each gate			upper limit A
Output load factor	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor	A-inputs	F_I	1
	strobe 1	F_I	4
	strobe 2	F_I	2

Logic $Q = \overline{A \text{ strobe}}$

FZH 211/215, Quadruple 2-Input NAND-Gate with Open Collector Output and N-Input
FZH 231/235 Dual 5-Input NAND-Gate with Open Collector Output and N-Input
Calculation of the collector resistance see FZH 161/165 and FZH 181/185

Electrical characteristics

12-V-range temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}	2			4.5	V
L-output voltage	V_{QL}	$V_S = V_{SB}$	1		0.9	1.7	V
		V_{IH}=7.5V, I_{QL}=15mA					
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input except N	I_{IH}	$V_S = V_{SA}$	3			1.0	µA
		$V_I = V_{IHA}$					
L-input current, each input except N	$-I_{IL}$	$V_S = V_{SA}$	4		0.8	1.5	mA
		V_{IL}=1.7 V					
H-output current, each output	I_{QH}	$V_S = V_{SB}$	8			80	µA
		V_{IL}=4.5V, V_{QH}=18V					
H-supply-current, each gate	I_{SH}	$V_S = V_{SA}$	6		1.0	1.7	mA
		V_I=0 V					
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$	7		0.4	1.0	mA
		$V_I = V_{IHA}$					
Power consumption, each gate	P	$V_S = V_{SA}$ duty cycle 1:1			8.5	18	mW

Delay times, V_S=12 V, T_A=25 °C

Propagation delay	t_{PLH}	V_{SC}=12 V	28	30	70	150	ns
	t_{PHL}	C_L=15 pF		90	175	310	ns
Transition time	t_{TLH}	R_C=760 Ω		120	230	450	ns
	t_{THL}			70	120	210	ns

Electrical characteristics

15-V-range
temperature ranges 1 and 5

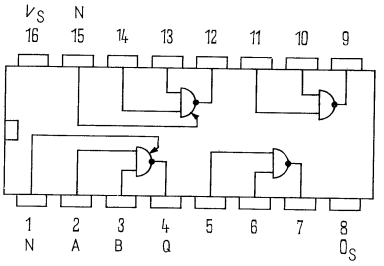
		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}	2			4.5	V
L-output voltage	V_{QL}	$V_S = V_{SB}$ $V_{IH} = 7.5$V, $I_{QL} = 18$mA	1		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input except N	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	3			1.0	µA
L-input current, each input except N	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	4		1.0	1.8	mA
H-output current, each output	I_{QH}	$V_S = V_{SB}$ $V_{IL} = 4.5$V, $V_{QH} = 18$V	8			80	µA
H-supply-current, each gate	I_{SH}	$V_S = V_{SA}$ $V_I = 0$ V	6		1.3	2.1	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$ $V_I = V_{IHA}$	7		0.7	1.4	mA
Power consumption, each gate	P	$V_S = V_{SA}$ duty cycle 1:1			15	30	mW

Delay times, $V_S = 15$ V, $T_A = 25$ °C

Propagation delay	t_{PLH}	$V_{SC} = 15$ V $C_L = 15$ pF $R_C = 760\,\Omega$	28				ns
	t_{PHL}						ns
Transition time	t_{TLH}						ns
	t_{THL}						ns

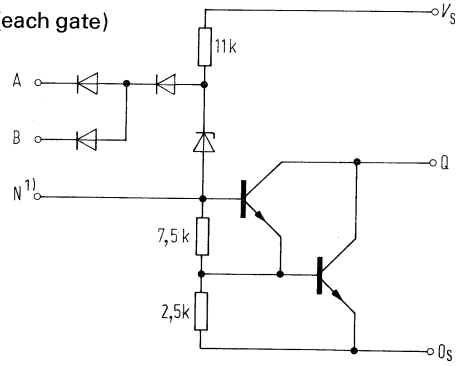
Quadruple 2-Input NAND-Gate with Open Collector Output and N-Input

Type	order numbers
FZH 211	Q 67000–H 639
FZH 215	Q 67000–H 640
FZH 231	Q 67000–H 642
FZH 235	Q 67000–H 643



Pin configuration
top view

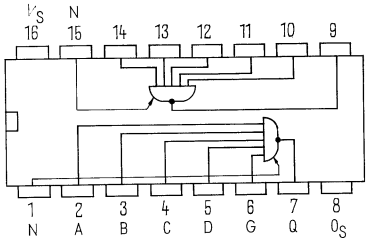
Schematic (each gate)



Logical data, each gate		upper limit A
L-Output load factor	F_{OL}	10
Input load factor, each input	F_I	1
Logic	$Q = \overline{AB}$	

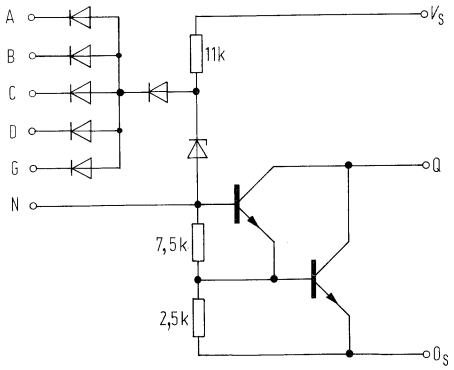
1) gates 1 and 4 only

Type	order numbers
FZH 211	Q 67000–H 639
FZH 215	Q 67000–H 640
FZH 231	Q 67000–H 642
FZH 235	Q 67000–H 643



Pin configuration
top view

Schematic (each gate)



Logical data, each gate		upper limit A
L-Output load factor	F_{QL}	10
Input load factor, each input	F_I	1

Logic $Q = \overline{ABCDG}$

Dual 4-Input NAND-Schmitt-Trigger with N-Input and Expander Nodes

FZH 241
FZH 245

Type	order numbers
FZH 241	Q 67000–H 645
FZH 245	Q 67000–H 646

The number of inputs can be expanded as required by means of additional input diodes BAW 76 at the expander input N_1. The anodes of the diodes must be connected in parallel to N_1.
If the supply is unregulated, it is recommended to use a decoupling capacitor of 1µF directly between pins 8 and 16.

Electrical characteristics

12 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}	2			4.5	V
Upper threshold voltage	V_{Tu}	V_S = 12.0 V	2		6.5		V
Lower threshold voltage	V_{Tl}	V_S = 12.0 V	2		5.6		V
Hysteresis	V_{HY}	V_S = 12.0 V	2		0.9		V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, V_{IL} = 4.5 V, $-I_{QH}$ = 0.1 mA	2	10.0	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, V_{IH} = 8.0V, I_{QL} = 15mA	1		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input except N	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	3			1.0	µA
L-input current, each input except N	$-I_{IL}$	$V_S = V_{SA}$, V_{IL} = 1.7 V	4			1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = V_Q$ = 0 V	5	9	15	25	mA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$, V_I = 0 V	6		4.0	6.3	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$, $V_I = V_{IHA}$	7		4.0	6.3	mA
Power consumption, each gate	P	$V_S = V_{SA}$, duty cycle 1:1			48	85	mW

Delay times, V_S = 12 V, F_Q = 1, T_A = 25 °C

Propagation delay	t_{PLH}	C_L = 10 pF at 4.5 V above ground	26	90	175	310	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}	C_L = 10 pF		200	340	570	ns
	t_{THL}			70	120	210	ns

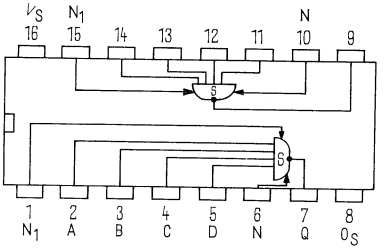
Electrical characteristics

15 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}	2			4.5	V
Upper threshold voltage	V_{Tu}	$V_S = 15.0$ V	2		6.4		V
Lower threshold voltage	V_{Tl}	$V_S = 15.0$ V	2		5.5		V
Hysteresis	V_{HY}	$V_S = 15.0$ V	2		0.9		V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA} $V_{IL} = 4.5$ V $-I_{QH} = 0.1$ mA	2	12.0	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$ $V_{IH} = 7.5$ V, $I_{QL} = 18$ mA	1		1.1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input except N	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	3			1.0	µA
L-input current, each input except N	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	4			1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$ $V_I = V_Q = 0$ V	5	9	15	25	mA
H-supply current, each gate	I_{SH}	$V_S = V_{SA}$ $V_I = 0$ V	6		4.5	7.3	mA
L-supply current, each gate	I_{SL}	$V_S = V_{SA}$ $V_I = V_{IHA}$	7		5.0	8.0	mA
Power consumption, each gate	P	$V_S = V_{SA}$ duty cycle 1:1			72	105	mW

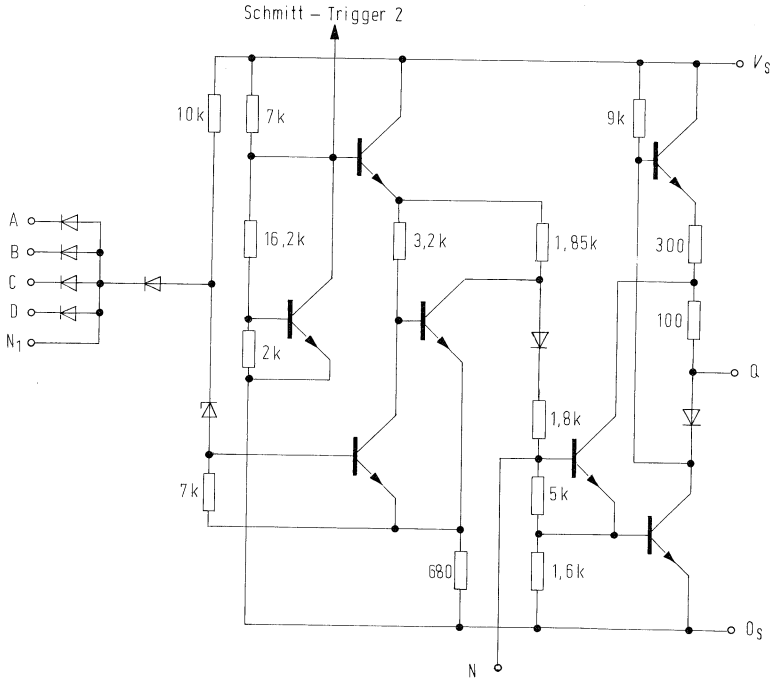
Delay times, $V_S = 15$ V, $F_Q = 1$, $T_A = 25$ °C

Propagation delay	t_{PLH}	$C_L = 10$ pF at 4.5 V above ground	26				ns
	t_{PHL}						ns
Transition time	t_{TLH}	$C_L = 10$ pF					ns
	t_{THL}						ns



Pin configuration
top view

Schematic (each gate)



Logical data, each gate			upper limit A
Output load factor	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1

Logic $Q = \overline{ABCDN_1}$

FZH 251/255 Quadruple 2-Input AND-Gate with N-Input
FZH 261/265 Dual 2-Input NAND-Gate and Quadruple Inverter
FZH 271/275 Quadruple 2-Input Exclusive-OR-Gate with N-Input
FZH 281/285 Quadruple 2-Input NOR-Gate with N-Input
FZH 291/295 Quadruple 2-Input OR-Gate with N-Input

Electrical Characteristics
12 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SA}$ and V_{SB}	2			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} $-I_{QH}=0.1$ mA	2	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $I_{QL}=15$ mA	1		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input except N	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	3			1.0	µA
I -input current, each input except N	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	4		0.8	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ $V_Q=0$ V	5	9	15	25	mA
Supply currents							
FZH 251/255							
H-supply current	I_{SH}	$V_I=V_{IHA}$ | $V_S=V_{SA}$	6		6.4	12.5	mA
L-supply current	I_{SL}	$V_I=0$ V | $V_S=V_{SA}$	7		9.6	18.0	mA
FZH 261/265							
H-supply current	I_{SH}	$V_I=0$ V | $V_S=V_{SA}$	6		6.2	12.5	mA
L-supply current	I_{SL}	$V_I=V_{IHA}$ | $V_S=V_{SA}$	7		10.2	18.0	mA
FZH 271/275							
H-supply current	I_{SH}	$V_{I1}=V_{IHA}$, $V_{I2}=0$V | $V_S=V_{SA}$	6		13.8	21.5	mA
L-supply current	I_{SL}	$V_I=0$ V | $V_S=V_{SA}$	7		15.2	24.0	mA
FZH 281/285							
H-supply current	I_{SH}	$V_I=0$ V | $V_S=V_{SA}$	6		13.2	21.5	mA
L-supply current	I_{SL}	$V_I=V_{IHA}$ | $V_S=V_{SA}$	7		14.8	24.0	mA
FZH 291/295							
H-supply current	I_{SH}	$V_I=V_{IHA}$ | $V_S=V_{SA}$	6		9.0	14.0	mA
L-supply current	I_{SL}	$V_I=0$ V | $V_S=V_{SA}$	7		14.4	24.0	mA

Electrical Characteristics

15 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SA}$ and V_{SB}	2			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA} $-I_{QH} = 0.1$ mA	2	12.0	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$ $I_{QL} = 18$ mA	1		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			4.6	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input except N	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	3			1.0	µA
L-input current, each input except N	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	4		1.0	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$ $V_Q = 0$ V	5	9	15	25	mA
Supply currents							
FZH 251/255							
H-supply current	I_{SH}	$V_I = V_{IHA}$ | $V_S = V_{SA}$	6		8.7	15.5	mA
L-supply current	I_{SL}	$V_I = 0$ V | $V_S = V_{SA}$	7		13.8	24.0	mA
FZH 261/265							
H-supply current	I_{SH}	$V_I = 0$ V | $V_S = V_{SA}$	6		8.2	14.5	mA
L-supply current	I_{SL}	$V_I = V_{IHA}$ | $V_S = V_{SA}$	7		14.4	24.0	mA
FZH 271/275							
H-supply current	I_{SH}	$V_{I1} = V_{IHA}$, $V_{I2} = 0$V | $V_S = V_{SA}$	6		16.4	24.0	mA
L-supply current	I_{SL}	$V_I = 0$ V | $V_S = V_{SA}$	7		19.2	30.0	mA
FZH 281/285							
H-supply current	I_{SH}	$V_I = 0$ V | $V_S = V_{SA}$	6		15.1	24.0	mA
L-supply current	I_{SL}	$V_I = V_{IHA}$ | $V_S = V_{SA}$	7		18.8	30.0	mA
FZH 291/295							
H-supply current	I_{SH}	$V_I = V_{IHA}$ | $V_S = V_{SA}$	6		10.5	18.5	mA
L-supply current	I_{SL}	$V_I = 0$ V | $V_S = V_{SA}$	7		18.4	30.5	mA

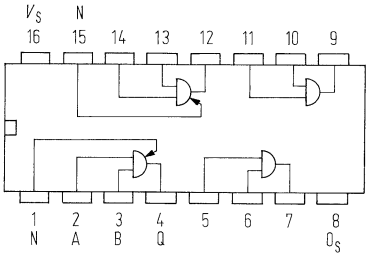
Delay times, V_S=12 V, F_Q=1, T_A=25 °C

FZH 261/265		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Propagation delay	t_{PLH}	C_L=10 pF at 4.5 V above ground	26	90	175	310	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}	C_L=10 pF		200	340	570	ns
	t_{THL}			70	120	210	ns
FZH 251/255, FZH 271/275, FZH 291/295							
Propagation delay	t_{PLH}	C_L=10 pF at 4.5 V above ground	26	200	340	570	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}	C_L=10 pF		200	340	570	ns
	t_{THL}			70	120	210	ns
FZH 281/285							
Propagation delay	t_{PLH}	C_L=10 pF at 4.5 V above ground	26	90	175	310	ns
	t_{PHL}			200	340	570	ns
Transition time	t_{TLH}	C_L=10 pF		200	340	570	ns
	t_{THL}			70	120	210	ns

Delay times, V_S=15 V, F_Q=1, T_A=25 °C

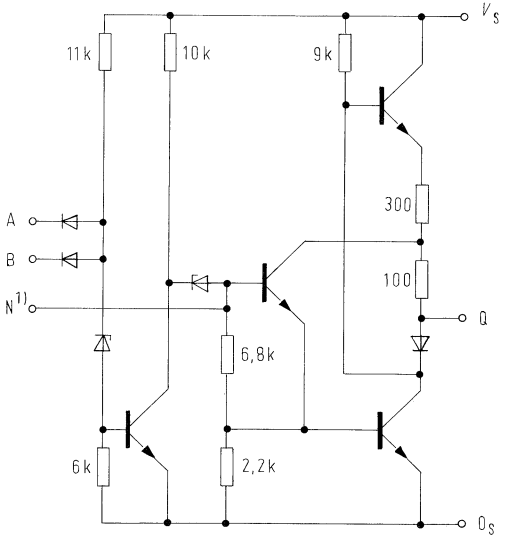
FZH 261/265							
Propagation delay	t_{PLH}	C_L=10 pF at 4.5 V above ground					ns
	t_{PHL}						ns
Transition time	t_{TLH}	C_L=10 pF					ns
	t_{THL}						ns
FZH 251/255, FZH 271/275, FZH 291/295							
Propagation delay	t_{PLH}	C_L=10 pF at 4.5 V above ground					ns
	t_{PHL}						ns
Transition time	t_{TLH}	C_L=10 pF					ns
	t_{THL}						ns
FZH 281/285							
Propagation delay	t_{PLH}	C_L=10 pF at 4.5 V above ground					ns
	t_{PHL}						ns
Transition time	t_{TLH}	C_L=10 pF					ns
	t_{THL}						ns

Type	order numbers
FZH 251	Q 67000–H 817
FZH 255	Q 67000–H 818



Pin configuration
top view

Schematic (each gate)

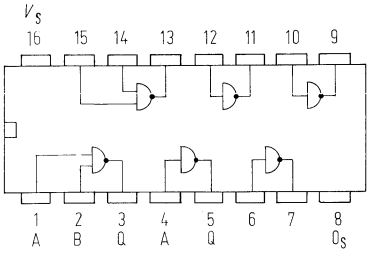


Logical data, each gate			upper limit A
Output load factor	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1

Logic $Q = AB$

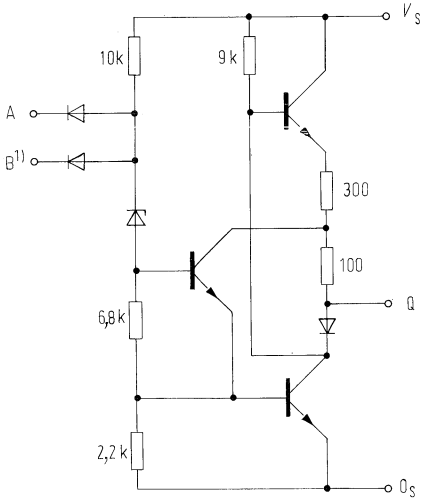
1) gates 1 and 4 only

Type	order numbers
FZH 261	Q 67000–H 819
FZH 265	Q 67000–H 820



Pin configuration
top view

Schematic (each gate)

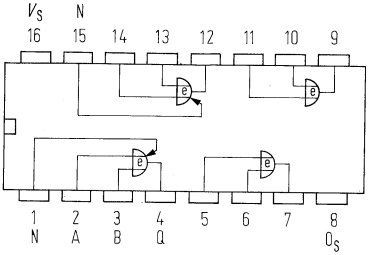


Logical data, each gate			upper limit A
Output load factor	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1

Logic gates 1 and 6 $Q = \overline{AB}$
gates 2, 3, 4, and 5 $Q = \overline{A}$

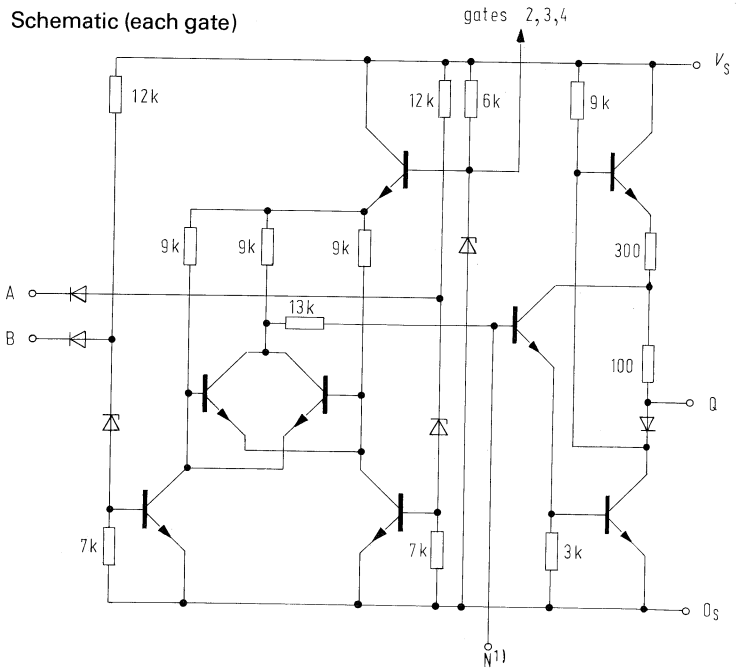
1) gates 1 and 6 only

Type	order numbers
FZH 271	Q 67000–H 821
FZH 275	Q 67000–H 822



Pin configuration
top view

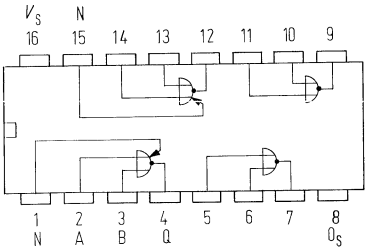
Schematic (each gate)



Logical data, each gate			upper limit A
Output load factor	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1
Logic			$Q = A\bar{B} + \bar{A}B$

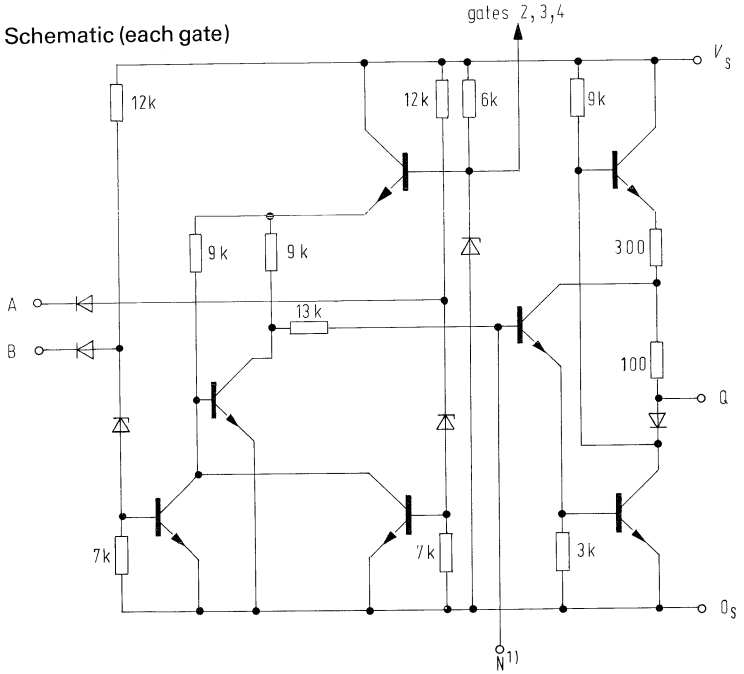
1) gates 1 and 4 only

Type	order numbers
FZH 281	Q67000-H823
FZH 285	Q67000-H824



Pin configuration
top view

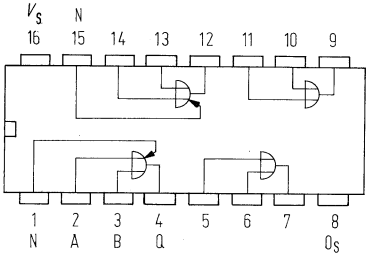
Schematic (each gate)



Logical data, each gate			upper limit A
Output load factor,	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1
Logic		$Q = \overline{A+B}$	

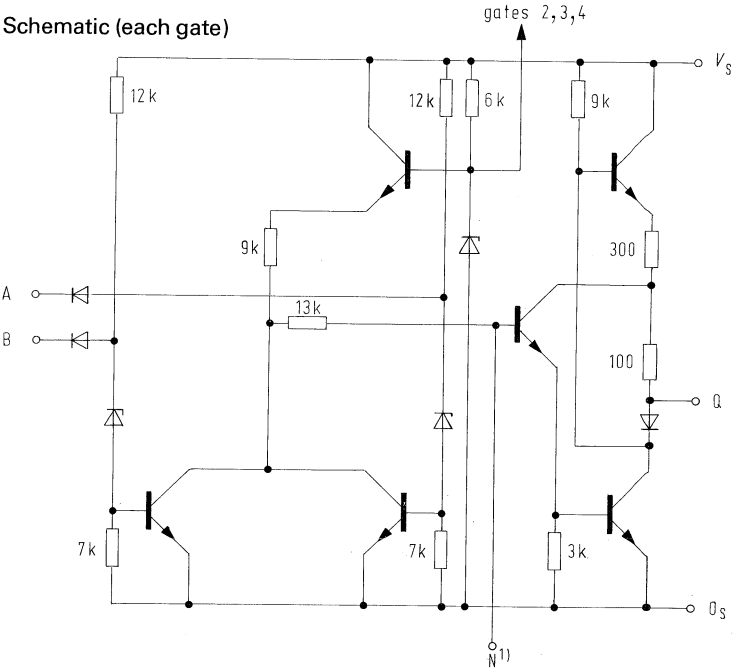
1) gates 1 and 4 only

Type	order numbers
FZH 291	Q 67000–H 825
FZH 295	Q 67000–H 826



Pin configuration
top view

Schematic (each gate)



Logical data, each gate			upper limit A
Output load factor,	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1
Logic			Q = *A*+*B*

1) gates 1 and 4 only

FZJ 101/105 JK-Master-Slave-Flipflop with two J and K-Inputs
FZJ 111/115 JK-Master-Slave Flipflop with N-Inputs

Type	order numbers
FZJ 101	Q 67000–J 95
FZJ 105	Q 67000–J 124
FZJ 111	Q 67000–J 96
FZJ 115	Q 67000–J 125

Electrical characteristics

12 V-range temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	22	7.5			V
L-input voltage at any input except C	V_{IL}	$V_S=V_{SB}$ and V_{SA}	22			4.5	V
L-input voltage at C	V_{IL}	$V_S=V_{SB}$ and V_{SA}	22			4.0	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} $V_{IL}=4.5$ V [1] $-V_{QH}=0.1$ mA	22	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V [1] $I_{QL}=15$ mA	22		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current at any input except C and N	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	23			1.0	µA
H-input current at C	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$	23			3.0	µA
L-input current at any input except C and N	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	24		0.8	1.5	mA
L-input current at C	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	24		1.6	3.0	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ $V_Q=0$ V	25	10.0	30.0	50.0	mA
Supply current	I_S	$V_S=V_{SA}$	23		8.0	14.0	mA

1) V_I applied to R and S resp.

Delay times, V_S=12 V, F_Q=1, T_A= 25 °C

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Maximum clock frequency	f	duty cycle 1:1		0.2	0.5		MHz
Clock pulse duration	t_{pC}			0.6			µs
Reset pulse duration	t_{pR}			1.0			µs
Set pulse duration	t_{pS}	at 50%		1.0			µs
Setup time	t_S			0			ns
Hold time	t_H			0			ns
Propagation delay from C to Q	t_{PLH}		31	160	290	520	ns
	t_{PHL}	C_L=10 pF at 4.5 V	31	270	450	770	ns
from $\overline{R}$ or $\overline{S}$ to Q	t_{PLH}	above ground	30	70	165	330	ns
	t_{PHL}		30	180	330	580	ns
Transition time	t_{TLH}	C_L=10 pF	31	200	340	570	ns
at Q	t_{THL}		31	70	120	210	ns

1) V, applied to $\overline{R}$ and $\overline{S}$ resp.

Electrical characteristics

15 V-range temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	22	7.5			V
L-input voltage at any input except C	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.5	V
L-input votage at C	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.0	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA} $V_{IL} = 4.5$ V [1] $-V_{QH} = 0.1$ mA	22	12.0	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$ $V_{IH} = 7.5$ V [1] $I_{QL} = 18$ mA	22		1.1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current at any input except C and N	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	23			1.0	µA
H-input current at C	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$	23			3.0	µA
L input current at any input except C and N	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	24		1.0	1.8	mA
L-input current at C	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	24		2.0	3.6	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$ $V_Q = 0$ V	25	15.0	37.0	60.0	mA
Supply current	I_S	$V_S = V_{SA}$	23		11.0	20.0	mA

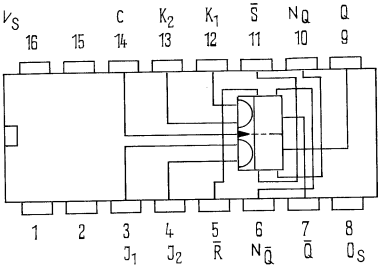
Delay times, $V_S = 15$ V, $F_Q = 1$, $T_A = 25$ °C

Propagation delay from C to Q	t_{PLH}	$C_L = 10$ pF at 4.5 V above ground	31		330		ns
	t_{PHL}		31		470		ns
from $\overline{R}$ or $\overline{S}$ to Q	t_{PLH}		30		195		ns
	t_{PHL}		30		340		ns
Transition time at Q	t_{TLH}	$C_L = 10$ pF	31		410		ns
	t_{THL}		31		75		ns

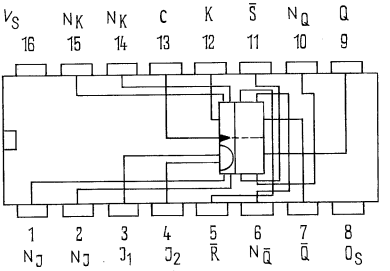
1) V, applied to $\overline{R}$ and $\overline{S}$ resp.

Pin configurations, top view

FZJ 101/105



FZJ 111/115



Logical data			upper limit A
Output load factor	H-signal	F_{QH}	100
each output	L-signal	F_{QL}	10
Input load factor at C	H-signal	F_{IH}	3
	L-signal	F_{IL}	2
remaining inputs		F_I	1

Note: $\bar{R}$ and $\bar{S}$ are approx. 1.5 normalized loads dynamically.

Truth table

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

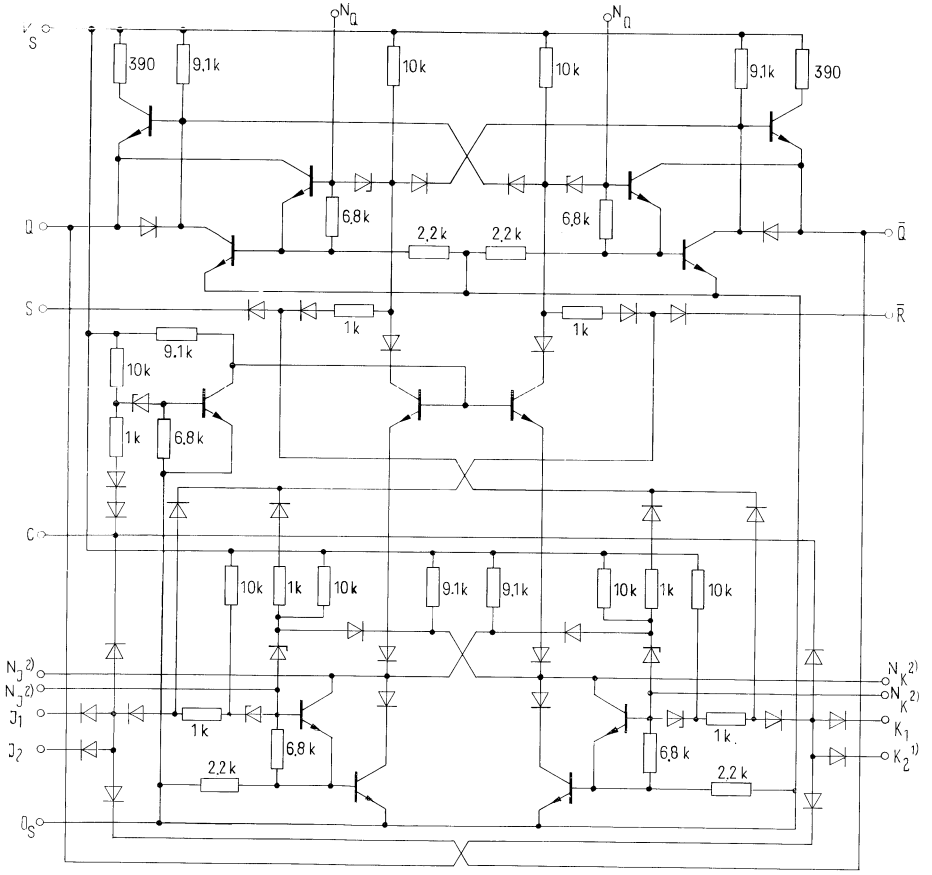
$J = J_1J_2$
$K = K_1K_2$ FZJ 101/115 only
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

L-level at $\bar{R}$ sets Q to L
L-level at $\bar{S}$ sets Q to H
$\bar{R}$ and $\bar{S}$ operate independently of C.

clock pulse

1 isolate slave from master
2 enter signal from J and K into master
3 disable inputs J and K
4 transfer information from master to slave

Schematic



C = clock, J, K = inputs, Q, $\overline{Q}$ = outputs, $\overline{R}$ = reset, $\overline{S}$ = set

1) FZJ 101/105 only 2) FZJ 111/115 only

Type	order numbers
FZJ 121	Q 67000–J 385
FZJ 125	Q 67000–J 386

Electrical characteristics

12 V-range
temperature range 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage at C	V_{IH}	$V_S = V_{SB}$	22	8.0			V
L-input voltage at C	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.0	V
H-input voltage at J and K	V_{IH}	$V_S = V_{SB}$	22	8.0			V
L-input voltage at J and K	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			5.5	V
H-input voltage at $\overline{R}$ and $\overline{S}$	V_{IH}	$V_S = V_{SB}$	22	7.5			V
L-input voltage at $\overline{R}$ and $\overline{S}$	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA} $V_{IL} = 4.5$ V [1] $-I_{QL} = 0.1$ mA	22	10.0	11.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$ $V_{IH} = 7.5$ V [1] $I_{QL} = 15$ mA	22		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			2.0	5.0		V
L-signal	V_{nm}			2.3	5.0		V
H-input current at C	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	23			3.0	µA
H-input current at J, K, $\overline{R}$ and $\overline{S}$	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	23			1.0	µA
L-input current at C	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	24		1.6	3.0	mA
L-input current at J, K, $\overline{R}$ and $\overline{S}$	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	24		0.8	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$ $V_Q = 0$ V	25	9.0	15.0	25.0	mA
Supply current	I_S	$V_S = V_{SA}$	23		15.0	24.0	mA

Delay times, V_S=12 V, F_Q=1, T_A= 25 °C

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Maximum clock frequency	f	duty cycle 1:1		0.2	0.5		MHz
Clock pulse duration	t_{pC}			0.6			s
Reset pulse duration	t_{pR}			1.0			s
Set pulse duration	t_{pS}	at 50%		1.0			s
Setup time	t_S			0			ns
Hold time	t_H			0			ns
Propagation delay from C to Q	t_{PLH}		31	160	290	520	ns
	t_{PHL}	C_L=10 pF at 4.5 V	31	270	450	770	ns
from $\overline{R}$ or $\overline{S}$ to Q	t_{PLH}	above ground	30	70	165	330	ns
	t_{PHL}		30	180	330	580	ns
Transition time	t_{TLH}	C_L=10 pF	31	200	340	570	ns
at Q	t_{THL}		31	70	120	210	ns

1) V, applied to $\overline{R}$ and $\overline{S}$ resp.

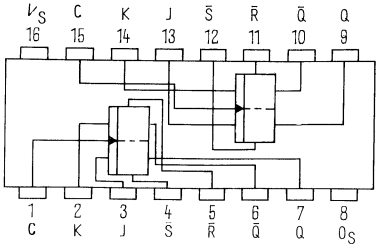
Electrical characteristics

15 V-range
temperature range 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage at C	V_{IH}	$V_S = V_{SB}$	22	8.0			V
L-input voltage at C	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.0	V
H-input voltage at J and K	V_{IH}	$V_S = V_{SB}$	22	8.0			V
L-input voltage at J and K	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			5.5	V
H-input voltage at $\overline{R}$ and $\overline{S}$	V_{IH}	$V_S = V_{SB}$	22	7.5			V
L-input voltage at $\overline{R}$ and $\overline{S}$	V_{IL}	$V_S = V_{SB}$ and V_{SA}	22			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA} $V_{IL} = 4.5$ V [1] $-I_{QL} = 0.1$ mA	22	12.0	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$ $V_{IH} = 7.5$ V [1] $I_{QL} = 18$ mA	22		1.1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.0	8.0		V
L-signal	V_{nm}			2.3	5.0		V
H-input current at C	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	23			3.0	µA
H-input current at J, K, $\overline{R}$ and $\overline{S}$	I_{IH}	$V_S = V_{SA}$ $V_I = V_{IHA}$	23			1.0	µA
L-input current at C	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	24		2.0	3.6	mA
L-input current at J, K, $\overline{R}$ and $\overline{S}$	$-I_{IL}$	$V_S = V_{SA}$ $V_{IL} = 1.7$ V	24		1.0	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$ $V_Q = 0$ V	25	9.0	15.0	25.0	mA
Supply current	I_S	$V_S = V_{SA}$	23		20.0	32.0	mA

Delay times, $V_S = 15$ V, $F_Q = 1$, $T_A = 25$ °C

Propagation delay from C to Q	t_{PLH}	$C_L = 10$ pF at 4.5 V above ground	31		330		ns
	t_{PHL}		31		470		ns
from $\overline{R}$ or $\overline{S}$ to Q	t_{PLH}		30		195		ns
	t_{PHL}		30		340		ns
Transition time at Q	t_{TLH}	$C_L = 10$ pF	31		410		ns
	t_{THL}		31		75		ns



Pin configuration
top view

Truth table

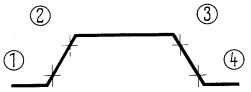
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
L-level at $\bar{R}$ sets Q to L.
L-level at $\bar{S}$ sets Q to H.
$\bar{R}$ and $\bar{S}$ operate independently of C.

Logical data, each flipflop			upper limit A
Output load factor	H-signal	F_{OH}	100
each output	L-signal	F_{OL}	10
Input load factor			
at C	H-signal	F_{IH}	3
at $\bar{R}$ and $\bar{S}$	H-signal	F_{IH}	1
at C, $\bar{R}$ and S	L-signal	F_{IL}	2
remaining inputs		F_I	1

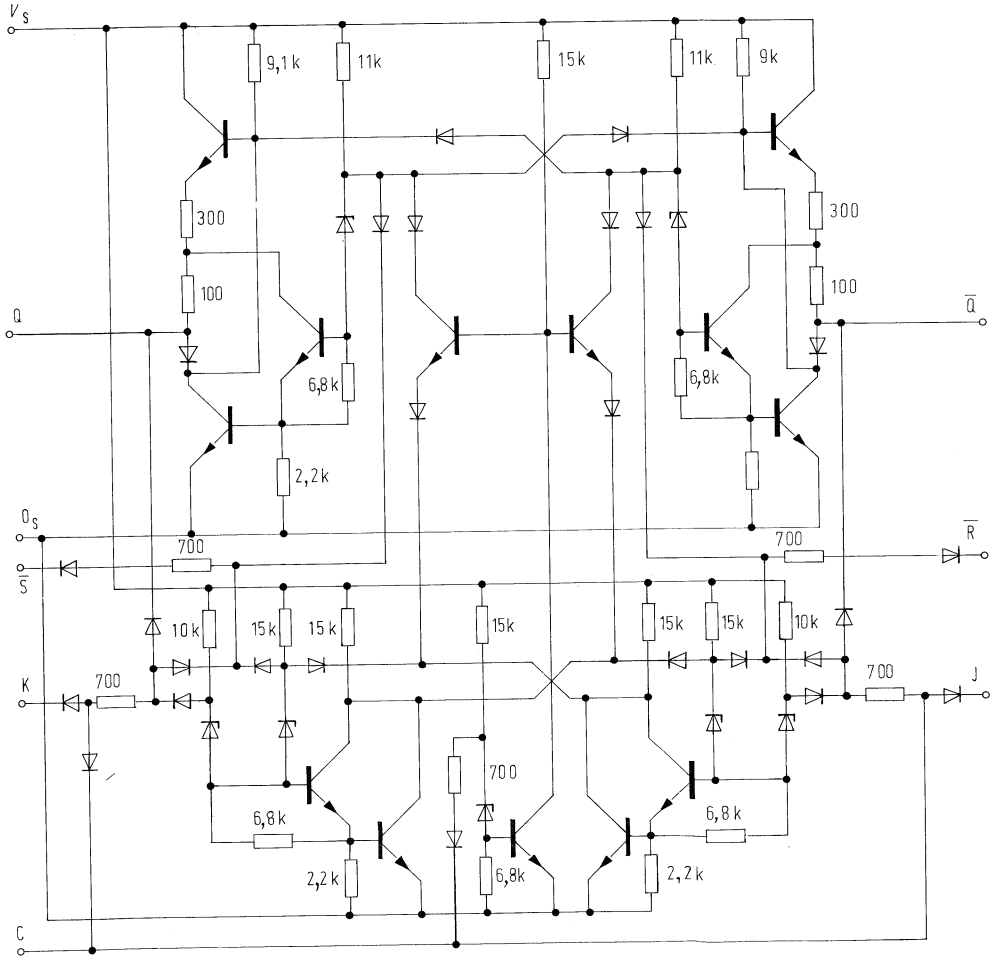
Note: $\bar{R}$ and $\bar{S}$ are approx. 1.5 normalized loads dynamically

Clock pulse



1 isolate slave from master
2 enter signal from J and K into master
3 disable inputs J and K
4 transfer information from master to slave

Schematic



C = clock, J, K = inputs, Q, $\overline{Q}$ = outputs, $\overline{R}$ = reset, $\overline{S}$ = set

Type	order numbers
FZJ 131	Q 67000-J 388
FZJ 135	Q 67000-J 389

The FZJ 131/135 contain four D-flipflops. Information present at the D-input is transferred to the Q-output while the clock input C is at H. The D-input is disabled at C = L.
Application: 4 bit scratch pad memory

Electrical characteristics

12 V-range
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$, $-I_Q=0.1$ mA $V_{IH}=7.5$ V	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$, $I_Q=15$ mA $V_{ID}=4.5$ V, $V_{IC}=7.5$ V		0.9	1.7	V
DC noise margin						
H-signal	V_{nm}		2.5	5		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input	I_I	$V_I=V_{IHA}$, $V_S=V_{SA}$			1	µA
L-input current at D	$-I_I$	$V_S=V_{SB}$, $V_I=1.7$ V			3	mA
L-input current at C	$-I_I$	$V_S=V_{SA}$, $V_I=1.7$ V			6	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$, $V_I=V_Q=0$ V	9	15	25	mA
Supply current	I_S	$V_S=V_{SA}$, $V_I=0$ V		22	32	mA
Power consumption	P	$V_S=V_{SA}$, $V_I=0$ V		264	432	mW

Delay times, V_S=12 V, F_Q=1, T_A=25 °C

		test condition	lower limit B	typ.	upper limit A	unit
Maximum clock frequency	f	duty cycle 1:1	0.5			MHz
Clock pulse duration	t_{pC}		0.5			s
Setup time at D						
H-signal	t_S		300			ns
L-signal	t_S	4.5 V above ground	500			ns
Hold time at D						
H-signal	t_H		150			ns
L-signal	t_H		50			ns
Propagation delay						
from D to Q	t_{PLH}		90	175	310	ns
	t_{PHL}		30	70	150	ns
from D to $\overline{Q}$	t_{PLH}		30	70	150	ns
	t_{PHL}	C_L= 10 pF at 4.5 V	70	130	290	ns
from C to Q	t_{PLH}	above ground	90	160	310	ns
	t_{PHL}		70	120	210	ns
from C to $\overline{Q}$	t_{PLH}		90	150	310	ns
	t_{PHL}		70	120	210	ns
Transition time	t_{TLH}	C_L = 10 pF	50	90	170	ns
	t_{THL}		15	35	60	ns

Electrical characteristics

15 V-range
temperature ranges 1 and 5

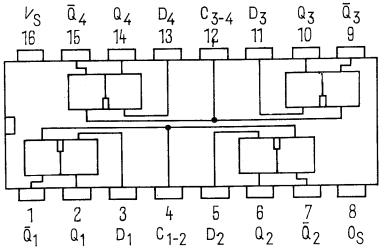
		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		13.5	15.0	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $-I_Q = 0.1$ mA, $V_{IH} = 7.5$ V	12.0	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_Q = 18$ mA, $V_{ID} = 4.5$ V, $V_{IC} = 7.5$ V		1.0	1.7	V
DC noise margin						
H-signal	V_{nm}		4.5	8		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input	I_I	$V_I = V_{IHA}$, $V_S = V_{SA}$			1	µA
L-input current at D	$-I_I$	$V_S = V_{SB}$, $V_I = 1.7$ V			3.6	mA
L-input current at C	$-I_I$	$V_S = V_{SA}$, $V_I = 1.7$ V			7.2	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = V_Q = 0$ V	9	15	25	mA
Supply current	I_S	$V_S = V_{SA}$, $V_I = 0$ V		28	42	mA
Power consumption	P	$V_S = V_{SA}$, $V_I = 0$ V		420	720	mW

Delay times, $V_S = 15$ V, $F_Q = 1$, $T_A = 25$ °C

Propagation delay						
from D to Q	t_{PLH}	$C_L = 10$ pF at 4.5 V above ground				ns
	t_{PHL}					ns
from D to $\overline{Q}$	t_{PLH}					ns
	t_{PHL}					ns
from C to Q	t_{PLH}					ns
	t_{PHL}					ns
from C to $\overline{Q}$	t_{PLH}					ns
	t_{PHL}					ns
Transition time	t_{TLH}	$C_L = 10$ pF				ns
	t_{THL}					ns

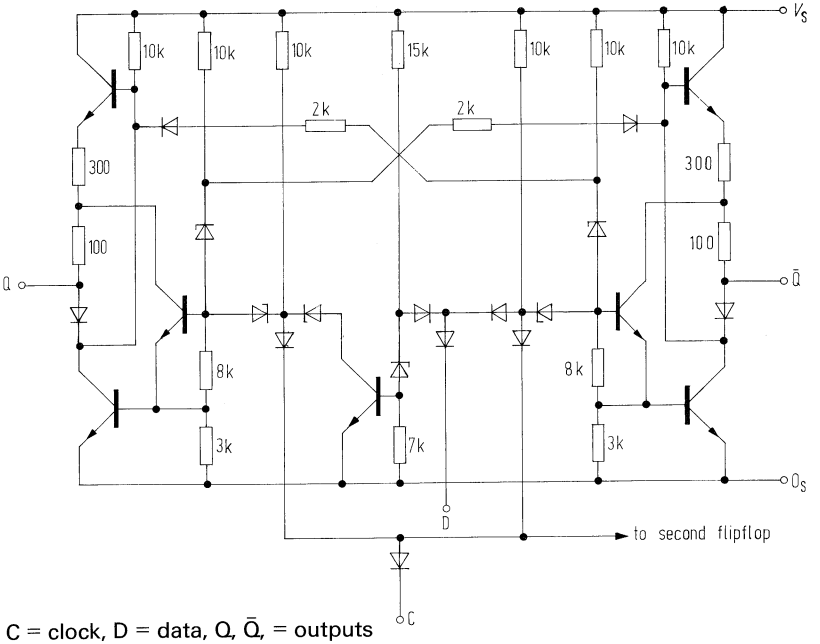
Logical data, each flipflop

Output load factor, H-signal	F_{QH}				100	
each output L-signal	F_{QL}				10	
Input load factor at D	F_I				2	
Input load factor at C	F_I	for 2 flipflops			4	



Pin configuration
top view

Schematic (each flipflop)



C = clock, D = data, Q, $\bar{Q}$, = outputs

Truth table (each flipflop)

inputs		output
C	D_n	Q_{n+1}
L	L	Q_n
L	H	Q_n
H	L	L
H	H	H

n: bit time before clock pulse
n + 1: bit time after clock pulse

FZJ 141/145 Synchronous Decimal Counter
FZJ 141A/145A Synchronous Decimal Counter with N-input
FZJ 151/155 Synchronous 4-Bit-Binary Counter
FZJ 151A/155A Synchronous 4-Bit-Binary Counter with N-input

Type	order numbers
FZJ 141	Q 67000-J 391
FZJ 145	Q 67000-J 392
FZJ 141 A	Q 67000-J 642
FZJ 145 A	Q 67000-J 647
FZJ 151	Q 67000-J 394
FZJ 155	Q 67000-J 395
FZJ 151 A	Q 67000-J 684
FZJ 155 A	Q 67000-J 685

The FZJ 141/145 and FZJ 151/155 are synchronous counters with set inputs for each bit, a common reset input, clock and carry gating. The information is stored in JK-flipflops. The information is transferred to the Q-outputs at the trailing edge of the clock pulse. The A-version is intended for application where the dynamic noise immunity must be increased. A delay capacitor may be added between N-input and ground in these cases. A synchronous counter chain is formed by connecting C_Q to E and E_C.

Electrical characteristics
12 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S = V_{SB}$		7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}				4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $-I_Q = 0.1$ mA		10.0	11.3		V
L-output voltage	V_{QH}	$V_S = V_{SB}$, $I_Q = 15$ mA			0.9	1.7	V
DC noise margin, H-signal	V_{nm}			2.5	5		V
L-signal	V_{nm}			2.8	5		V
H-input current, each input except N	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$				1	µA
L-input current, each input except N	$-I_{IL}$	$V_S = V_{SA}$, $V_I = 1.7$ V			0.8	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0$ V		9	15	25	mA
H-supply current	I_{SH}	$V_S = V_{SA}$, $V_I = V_{SA}$			12	17	mA
L-supply current	I_{SL}	$V_S = V_{SA}$ input $\overline{R}$: $V_I = 0$ V remaining inputs: $V_I = V_{SA}$			20	29	mA

Delay times, V_S=12 V, F_Q=1, T_A=25 °C

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Capacitance	C_N			0		1	nF
Maximum clock frequency	f	duty cycle 1 :1		0.5	1.5		MHz
Clock pulse duration	t_{pC}			0.5			µs
Reset pulse duration	t_{pR}			0.5			µs
Reset recovery time	t_{rR}		53			2	µs
referred to the HL clock pulse transition		4.5 V above ground					
Reset pulse duration during set operation	t_{pR}		54	1			µs
Setup time at $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$	t_S		54	1			µs
Hold time at $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$	t_H		54	1			µs
Propagation delay from C to Q	t_{PLH}			90	200	450	ns
	t_{PHL}		50	90	200	450	ns
from C to C_Q	t_{PLH}			200	400	700	ns
	t_{PHL}			150	300	500	ns
from E_C to C_Q	t_{PLH}	C_L = 10 pF at	52	90	200	450	ns
	t_{PHL}	4.5 V above ground	52	25	60	200	ns
from $\overline{R}$ to Q	t_{PHL}		53	70	150	310	ns
from $\overline{A}$ to Q_A, $\overline{B}$ to Q_B,	t_{PLH}		51	30	120	210	ns
$\overline{C}$ to Q_C, $\overline{D}$ to Q_D	t_{PHL}		51	30	120	210	ns
Transition times							
at C	t_T			1			V/µs
at Q	t_{TLH}			90	250	450	ns
	t_{THL}	C_L = 10 pF	50	5	20	60	ns
at C_Q	t_{TLH}			70	140	310	ns
	t_{THL}			30	60	210	ns

Electrical characteristics

15 V-range
temperature ranges 1 and 5

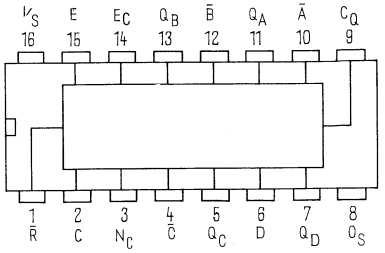
		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15	17.0	V
H-input voltage	V_{IH}	$V_S = V_{SB}$		7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}				4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $-I_Q = 0.1$ mA		12	14.3		V
L-output voltage	V_{QH}	$V_S = V_{SB}$, $I_Q = 18$ mA			1	1.7	V
DC noise margin, H-signal	V_{nm}			4.5	8		V
L-signal	V_{nm}			2.8	5		V
H-input current, each input except N	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$				1	µA
L-input current, each input except N	$-I_{IL}$	$V_S = V_{SA}$, $V_I = 1.7$ V			1	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0$ V		9	15	25	mA
H-supply current	I_{SH}	$V_S = V_{SA}$, $V_I = V_{SA}$			15	23	mA
L-supply current	I_{SL}	$V_S = V_{SA}$ input $\overline{R}$: $V_I = 0$ V remaining inputs: $V_I = V_{SA}$			23	36.5	mA

Delay times, $V_S = 15$ V, $F_Q = 1$, $T_A = 25$ °C

Propagation delay from C to Q	t_{PLH}	C_L = 10 pF at 4.5 V above ground	50				ns
	t_{PHL}						ns
from C to C_Q	t_{PLH}						ns
	t_{PHL}						ns
from E_C to C_Q	t_{PLH}		52				ns
	t_{PHL}		52				ns
from $\overline{R}$ to Q	t_{PHL}		53				ns
from $\overline{A}$ to Q_A, $\overline{B}$ to Q_B,	t_{PLH}		51				ns
$\overline{C}$ to Q_C, $\overline{D}$ to Q_D	t_{PHL}		51				ns
Transition times							
at C	t_T	C_L = 10 pF					V/µs
at Q	t_{TLH}						ns
	t_{THL}		50				ns
at C_Q	t_{TLH}						ns
	t_{THL}						ns

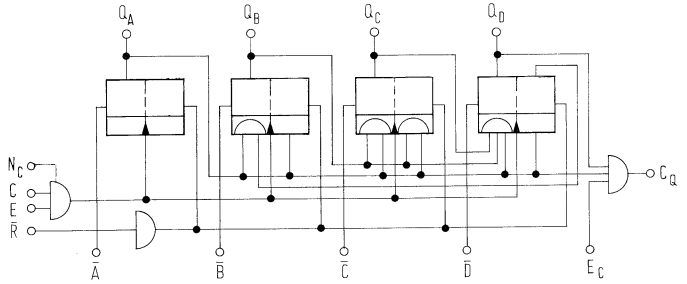
Logical data

Output load factor H-signal	F_{QH}		100
each output L-signal	F_{QL}		10
Input load factor, each input	F_I		1

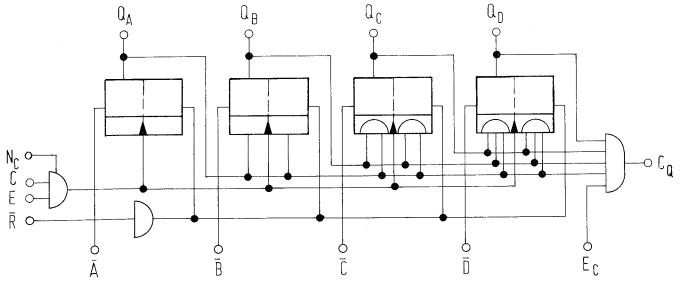


Pin configuration, top view
$\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$ = set inputs
C = clock input
C_Q = carry output
E = enable input
$\overline{R}$ = reset input
Q, $\overline{Q}$ = outputs

Block diagram of FZJ 141/145, FZJ 141 A/145 A
N_C-terminal FZJ 141 A/145 A only



Block diagram of FZJ 151/151, FZJ 151 A/155 A
N_C-terminal FZJ 151 A/155 A only



Truth table: Decimal counter
FZJ 141/145, FZJ 141 A/145 A

count condition: $\overline{A}=\overline{B}=\overline{C}=\overline{D}=\overline{E}=E_C=\overline{R}=H$

sequence	outputs C_Q	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	H	H	L	L	H

Truth table: Binary counter
FZJ 151/155, FZJ 151 A/155 A

count condition: $\overline{A}=\overline{B}=\overline{C}=\overline{D}=\overline{E}=E_C=\overline{R}=H$

sequence	outputs C_Q	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	H	H	H	H	H

Enable conditions

enable E	operating mode
L	inhibit
H	count

enable E_C	Carry output C_Q
L	L
H	L or H

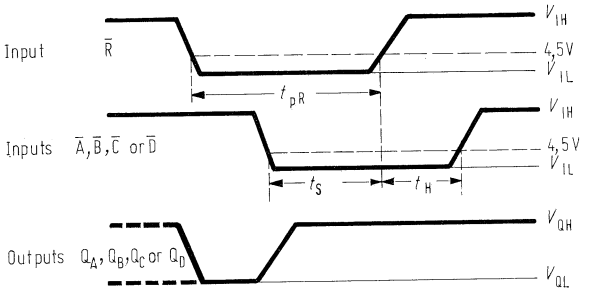
Set and reset conditions

Set and reset inputs operate independently of the clock input C and the enable input E. If these inputs are not used, they must be connected to V_S. To store the information properly $\overline{R}$ must return to H-level before the inputs $\overline{A}$ through $\overline{D}$.

inputs					outputs			
$\overline{R}$	$\overline{A}$	$\overline{B}$	$\overline{C}$	$\overline{D}$	Q_A	Q_B	Q_C	Q_D
L	H	H	H	H	L	L	L	L
L	L	X	X	X	H	X	X	X
L	X	L	X	X	X	H	X	X
L	X	X	L	X	X	X	H	X
L	X	X	X	L	X	X	X	H

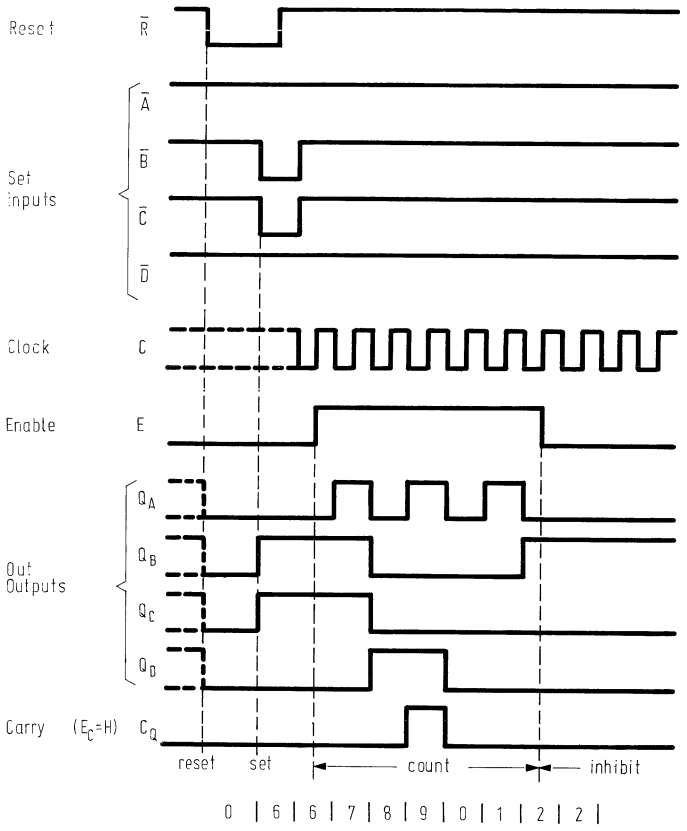
X = L or H-signal

Pulse diagram for set operation



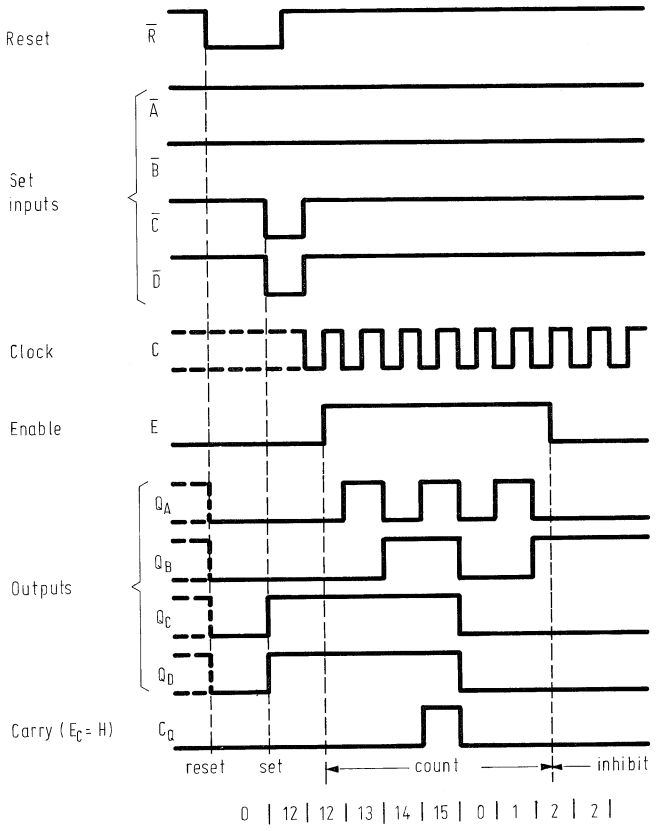
Pulse Diagram for the Decimal Counter with the following Sequence

1. Reset to Q = L
2. Set to binary 6
3. Count from binary 6 to 2 with carry pulse
4. Inhibit



Pulse Diagram for the Binary Counter with the following Sequence

1. Reset to Q = L
2. Set to binary 12
3. Count from binary 12 to 2 with carry pulse
4. Inhibit



Type	order numbers
FZJ 161	Q 67000-J 507
FZJ 165	Q 67000-J 562

The FZJ 161/165 are 4-bit-shiftregisters with serial and parallel inputs and outputs for right shift operation. The flipflops are set to their initial states by means of the set input S. A, B, C, and D are enabled at S = H. S and the reset input $\overline{R}$ operate independently of the clock puise. To increase the noise immunity of the serial input and the clock input respectively, a delay capacitor each can be connected between the respective N-inputs and ground. Applications: Serial register, parallel register, parallel-serial converter and serial-parallel converter.

Electrical characteristics

12 V-range temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$, $-I_Q=0.1$ mA $V_{IL}=4.7$ V	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$, $I_Q=15$ mA		0.9	1.7	V
DC noise margin						
H-signal	V_{nm}		2.5	5		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input except N	I_I	$V_I=V_{IHA}$, $V_S=V_{SA}$			1	µA
L-input current, each input except N and S	$-I_I$	$V_S=V_{SB}$, $V_I=1.7$ V			1.5	mA
L-input current at S	$-I_I$	$V_S=V_{SA}$, $V_I=1.7$ V			6	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$, $V_I=V_Q=0$ v	9	15	25	mA
Supply current	I_S	$V_S=V_{SA}$, $V_I=0$ V		21	33	mA
Power consumption	P	$V_S=V_{SA}$, $V_I=0$ V		180	340	mW

Delay times, V_S=12 V, F_Q=1, T_A=25 °C

		test condition	lower limit B	typ.	upper limit A	unit
Capacitance	C_N		0		1	nF
Maximum clock frequency	f	duty cycle 1 : 1	0.5	1.5		MHz
Clock pulse duration	t_{pC}		0.5			µs
Reset pulse duration	t_{pR}		0.5			µs
Reset pulse duration during set operation	t_{pR}	4.5 V above ground	1			µs
Setup time at A, B, C, D, S	t_H		1			µs
at SI	t_H		0			µs
Hold time at A, B, C, D, S	t_H		1			µs
at SI	t_V		0,5			µs
Propagation delay from CI to Q	t_{PLH}		90	140	450	ns
	t_{PHL}		90	140	450	ns
from $\overline{R}$ to Q	t_{PHL}	C_L=10 pF at	0.6	0.85	1.3	µs
from S to Q, A to Q_A, B to Q_B,	t_{PLH}	4.5 V above ground	100	240	500	ns
C to Q_C, D to Q_D	t_{PHL}		90	140	450	ns
Transition times at CI	t_T		1			V/µs
at Q	t_{TLH}	C_L=10 pF	70	150	290	ns
	t_{THL}		5	20	60	ns

Electrical characteristics

15 V-range
temperature ranges 1 and 5

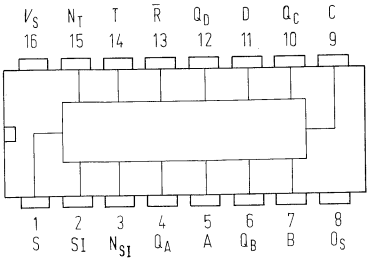
		test condition	lower limit B	typ	upper limit A	unit
Supply voltage	V_S		13.5	15	17	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$, $-I_Q = 0.1$ mA, $V_{IL} = 4.7$ V	12.0	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_Q = 18$ mA		1.0	1.7	V
DC noise margin						
H-signal	V_{nm}		4.5	8		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input except N	I_I	$V_I = V_{IHA}$, $V_S = V_{SA}$			1	µA
L-input current, each input except N and S	$-I_I$	$V_S = V_{SB}$, $V_I = 1.7$ V			1.8	mA
L-input current at S	$-I_I$	$V_S = V_{SA}$, $V_I = 1.7$ V			7.2	mA
Short circuit output current, each output	$-I_Q$	$V_S = V_{SA}$, $V_I = V_Q = 0$V	9	15	25	mA
Supply current	I_S	$V_S = V_{SA}$, $V_I = 0$ V		26	42	mA
Power consumption	P	$V_S = V_{SA}$, $V_I = 0$ V		390	715	mW

Delay times, $V_S = 15$ V, $F_Q = 1$, $T_A = 25$ °C

Propagation delay from CI to Q	t_{PLH}	$C_L = 10$ pF at 4,5 V above ground				ns
	t_{PHL}					ns
from $\overline{R}$ to Q	t_{PHL}					µs
from S to Q, A to Q_A, B to Q_B,	t_{PLH}					ns
C to Q_C, D to Q_D	t_{PHL}					ns
Transition times						
at CI	t_T	$C_L = 10$ pF				V/µs
at Q	t_{TLH}					ns
	t_{THL}					ns

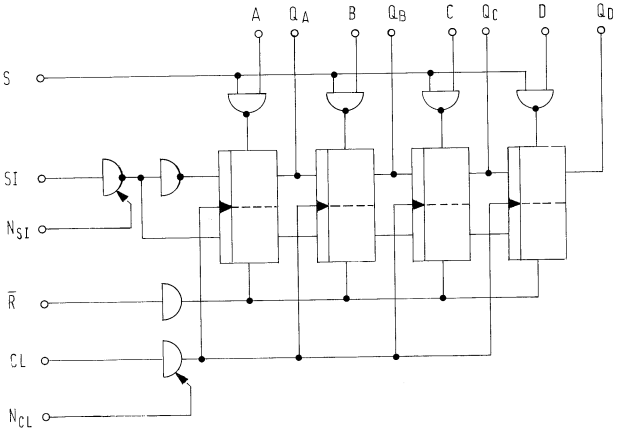
Logical data

Output load factor, H-signal	F_{QH}				100	
each output L-signal	F_{QL}				10	
Input load factor						
at S	F_I				4	
remaining inputs	F_I				1	



Pin cinfiguration, top view
A, B, C, D = inputs
CI = clock input
Q = outputs
$\overline{R}$ = reset input
S = set input
SI = serial input

Block diagram



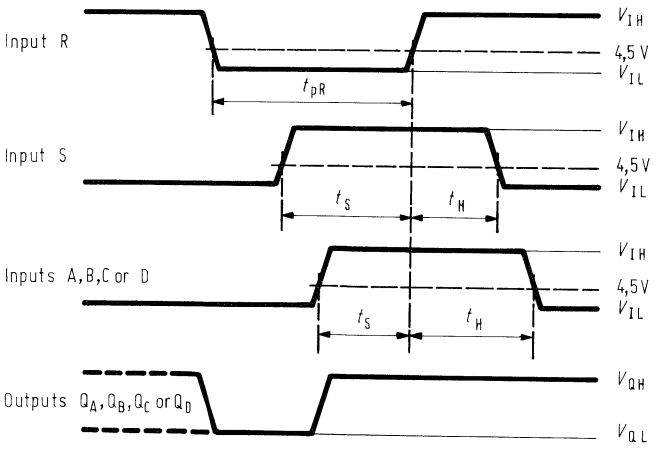
Set and reset conditions

Set and reset inputs operate independent of the clock input CL. To store the parallel information properly $\overline{R}$ must return to H-level before S is switched to L-level.

inputs						outputs			
S	$\overline{R}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	L	X	X	X	X	L	L	L	L
H	L	H	L	H	H	H	L	H	H
L	H	X	X	X	X	shift			

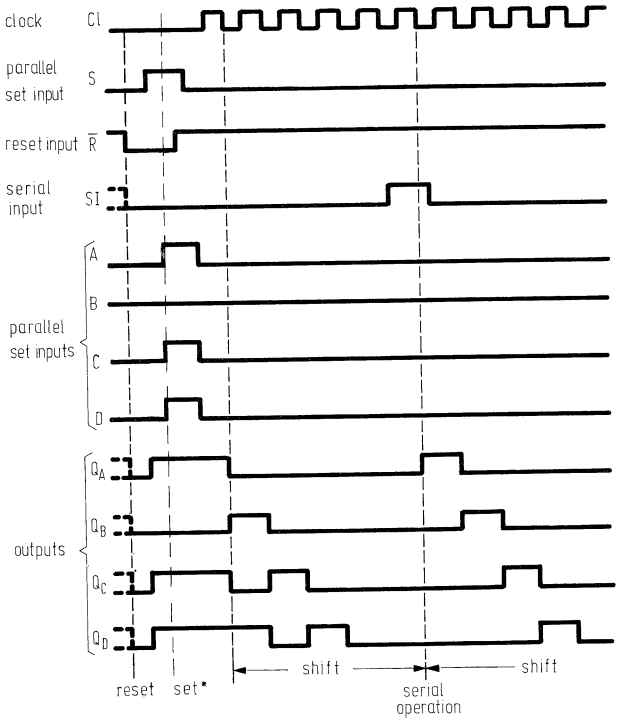
X = L or H-signal

Pulse diagram for set operation



Pulse Diagram with the following sequence

1. Reset to Q = L
2. Set to binary 13
3. Shift
4. Serial operation
5. Shift



* A falling clock transistion must not occur during parallel set operation

Type	order numbers
FZK 101	Q 67000–K 6
FZK 105	Q 67000–K 7

The FZK 101/105 feature the following operating modes:

1. Monostable multivibrator. L, J, and M connected.
2. Pulse delay. L and K connected.
3. Pulse reduction. J and M connected.
4. Delay switch, L-K and M-O_S connected.
5. Pulse delay is retriggerable if the retrigger pulse returns before the recovery time is elapsed.
6. An electrolytic capacitor can be used as timing component C_t.
7. Q remains at L only if $\overline{R}$ is supplied with an L-level after the supply voltage V_S is applied.
8. No voltages and currents may be applied to the function inputs J, K, L, M. The required connection between J, K, L, M may not exceed 5 mm.
9. Inputs A or B must be supplied with an L-level, if C and D are used as trigger inputs.
10. The delay capacitor is connected between N-input and ground.

Electrical characteristics

12 V-range
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} $V_{IL}=4.5$ V, $-I_{QH}=0.1$ mA	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V, $I_{QL}=15$mA		1.0	1.7	V
DC noise margin						
H-signal	V_{nm}		2.5	5.0		V
L-signal	V_{nm}		2.8	5.0		V
H-input current, each input	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$			1.0	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$, $V_{IL}=1.7$ V		0.8	1.5	mA
Short circuit output current	$-I_Q$	$V_S=V_{SA}$, $V_Q=0$	9	15	25	mA
L-supply current	I_{SL}			13	19	mA
H-supply current	I_{SH}			12	19	mA

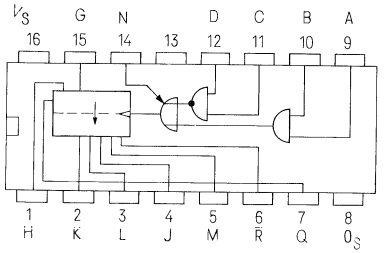
Electrical characteristics

15 V-range
temperature ranges 1 and 5

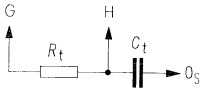
		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S = V_{SB}$ and V_{SA}, $V_{IL} = 4.5$ V, $-I_{QH} = 0.1$ mA	12.0	14.3		V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $V_{IH} = 7.5$ V, $I_{QL} = 18$ mA		1.1	1.7	V
DC noise margin						
H-signal	V_{nm}		4.5	8.0		V
L-signal	V_{nm}		2.8	5.0		V
H-input current, each input	I_{IH}	$V_S = V_{SA}$, $V_I = V_{IHA}$			1.0	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_{IL} = 1.7$ V		1.0	1.8	mA
Short circuit output current	$-I_Q$	$V_S = V_{SA}$, $V_Q = 0$	9	15	25	mA
L-supply current	I_{SL}			14	22	mA
H-supply current	I_{SH}			15	23	mA

Delay times, $V_S = 12$ V, $F_Q = 1$, $T_A = 25$ °C

Input pulse duration	t_{pI}		0.5			µs
Reset pulse duration	t_{pR}		0.5			µs
Setup time at A, B	t_S		0			µs
Setup time at C, D	t_S		0.5			µs
Recovery time	t_r		$(C_0 + C_t) \times 10^3$			s/F
Min. output pulse duration	t_p		400			ns
Output pulse duration	t_p	$V_S = 11.4$ V, $R_t = 0.5$ kΩ, $C_t = 2$ nF	650	700	780	ns
Propagation delay from A, B, C, D to Q	t_{PLH}	$C_L = 10$ pF at 4.5 V above ground	220	270	740	ns
	t_{PHL}		110	180	450	ns
from $\overline{R}$ to Q	t_{PHL}		150	300	550	ns
Transition times						
at A, B	t_{TLH}		0.1			V/µs
at C, D	t_{THL}		1			V/µs
at Q	t_{THL}	$C_L = 10$ pF	50	100	200	ns
	t_{THL}		30	80	150	ns



Pin configuration
top view



Logical data			upper limit A
Output load factor	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1
Logic			Q = (AB) + ($\overline{CD}$) see pulse diagram

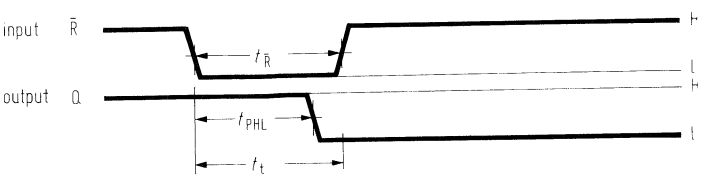
Truth table

inputs				output
A	B	C	D	Q
L	X	H	H	L
X	L	H	H	L
H	H	X	X	L
X	X	L	X	L
X	X	X	L	L
⌐	H	H	H	⌐¬
H	⌐	H	H	⌐¬
L	X	¬	H	⌐¬
L	X	H	¬	⌐¬
X	L	¬	H	⌐¬
X	L	H	¬	⌐¬

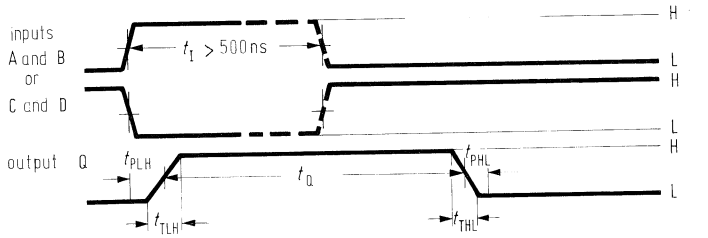
notes

X = L or H-signal
⌐¬ = H-pulse with adjustable duration
⌐ = L-H-transition
¬ = H-L-Transition
Output Q refers to operation as monostable multivibrator. It applies accordingly for the remaining operating modes.

Pulse diagrams for:

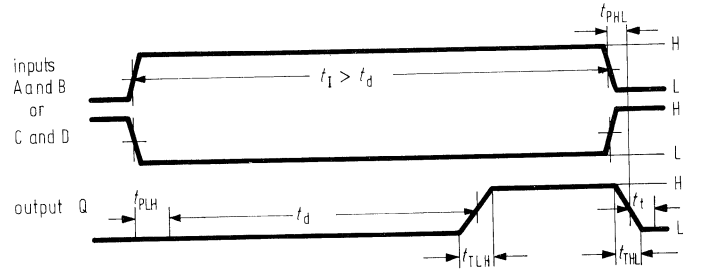


reset mode (applies for every operating mode)



monostable multivibrator (L, J, and M connected)

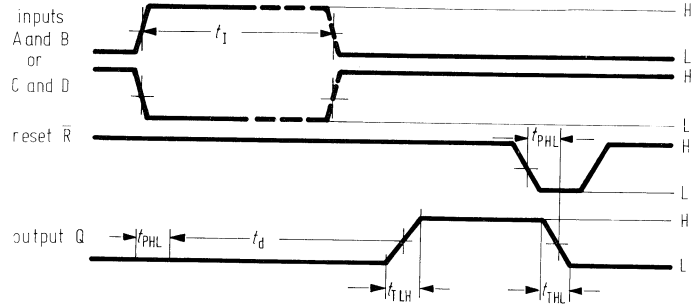
$t_Q = 0.7 \cdot R_t \cdot (C_0 + C_1)$



Pulse delay
(L and K connected)

$t_d = 0.7 \cdot R_t \cdot (C_0 + C_t)$

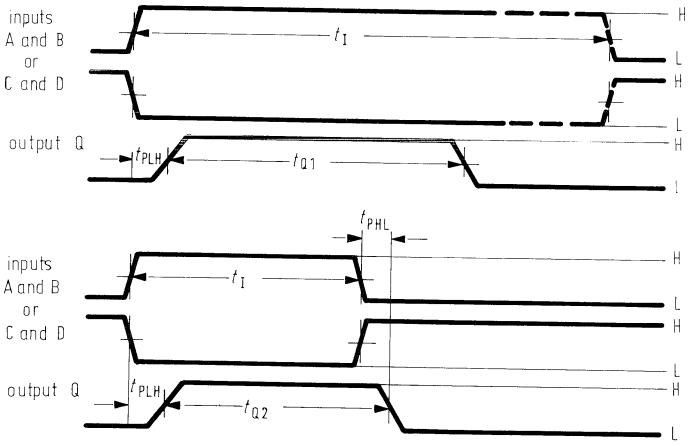
Pulse diagrams for:



Delay switch
(L-K and M-O_s connected)

Reset to Q=L by means of R= L only

$t_d = 0.7 \cdot R_t \cdot (C_0 + C_t)$



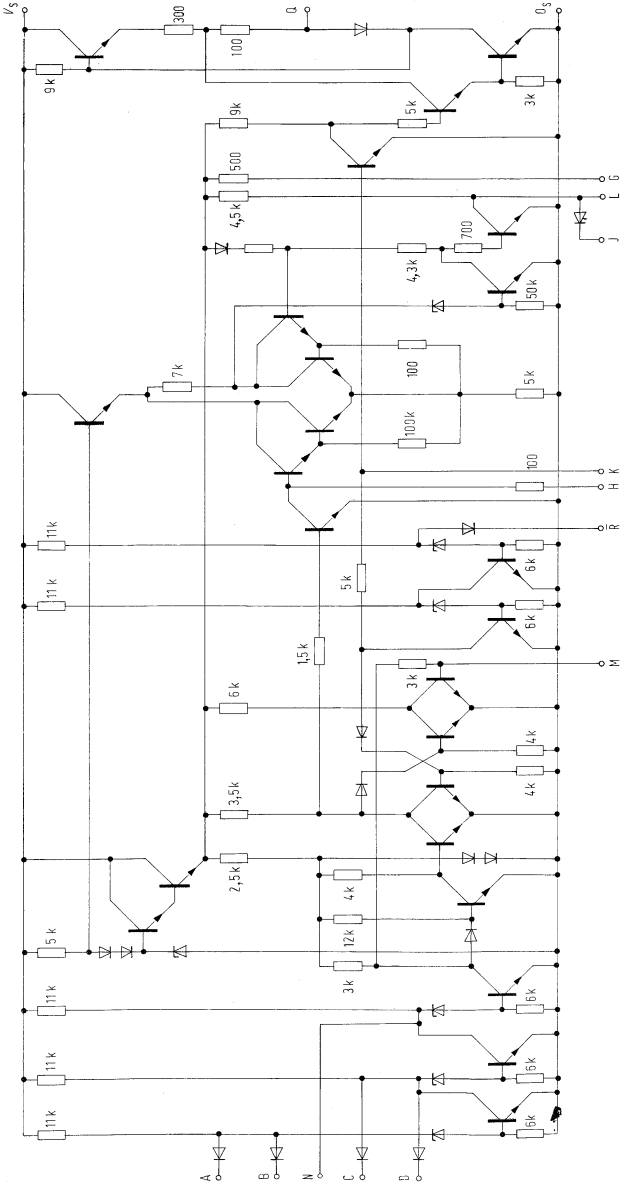
Pulse reduction
(J and M connected)
a) $t_I > 0.7 \cdot R_t \cdot (C_0 + C_t)$

$t_{Q1} = 0.7 \cdot R_t \cdot (C_0 + C_t)$

b) $t_I \leqq 0.7 \cdot R_t \cdot (C_0 + C_t)$

$t_{Q2} = t_I$

Schematic


V_S
300
100
Q
Q_S
9k
3k
5k
9k
500
4,5k
4,3k
700
50k
7k
100
5k
100k
100
11k
6k
5k
1,5k
3k
6k
4k
3,5k
2,5k
12k
A
B
N
C
D
G
L
J
K
H
M
R

Type	order numbers
FZL 101	Q 67000–L 68

The FZL 101 decodes binary coded decimal numbers. Direct control of indicator tubes is possible by means of output transistors with high breakdown voltages. The FZJ 141 is the corresponding decimal counter. The following connections have to be made from the Q-outputs of the FZJ 141 to the inputs of the FZL 101: Q_A to A, Q_B to B, Q_C to C, and Q_D to D. Binary input information of the decimal numbers 10 through 15 are suppressed.
In addition the following maximum ratings apply:

In addition the following maximum ratings apply:		lower limit B	upper limit A	unit
Output voltage (output transistor blocked)	V_Q	0	65	V
Output current (output transistor blocked), each output	I_Q	0	2	mA
Output current (output transistor conducting), each output	I_Q	0	20	mA

Electrical characteristics 12 V-range temperature range 1		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	8.0			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			5.0	V
L-output voltage	V_{QL}	$V_S=V_{SB}$, $I_{QL}=9$ mA			2.5	V
DC noise margin, H-signal	V_{nm}		2.0	4.5		V
L-signal	V_{nm}		3.3	5.5		V
H-output current, each output	I_Q	$V_S=V_{SA}$, $V_Q=65$ V			100	µA
	I_Q	$V_S=V_{SA}$, $V_Q=60$ V			5	µA
H-input current, each input	I_{IH}	$V_S=V_I=V_{SA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$, $V_I=0$ V		0.8	1.5	mA
Supply current	I_S	$V_S=V_{SA}$ input A, C, D: $V_I=0$ V		17	25	mA
Power consumption	P	input B: $V_I=V_{SA}$		205	340	mW

Delay times, $V_S=12$ V, $T_A=25$ °C

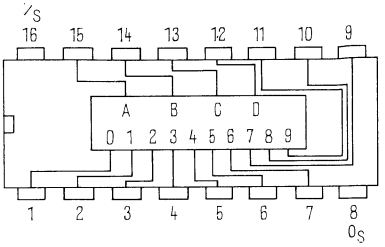
Propagation delay from B to dec 2	t_{PLH}	$V_{SC}=12$ v, $R_C=1$ kΩ, $C_L=10$ pF	30	70	210	ns
	t_{PHL}		60	150	280	ns
from B to dec 0	t_{PLH}		60	150	280	ns
	t_{PHL}		30	70	210	ns

Electrical characteristics
15 V-range
temperature range 1

		test condition	lower limit B	typ	upper limit A	unit
Supply voltage	V_S		13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S = V_{SB}$	8.0			V
L-input voltage	V_{IL}	$V_S = V_{SB}$ and V_{SA}			5.0	V
L-output voltage	V_{QL}	$V_S = V_{SB}$, $I_{QL} = 9$ mA			2.5	V
DC noise margin, H-signal	V_{nm}		4.0	7.5		V
L-signal	V_{nm}		3.3	5.5		V
H-output current, each output	I_Q	$V_S = V_{SA}$, $V_Q = 65$ V			100	µA
	I_Q	$V_S = V_{SA}$, $V_Q = 60$ V			5	µA
H-input current, each input	I_{IH}	$V_S = V_I = V_{SA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S = V_{SA}$, $V_I = 0$ V		1	1.8	mA
Supply current	I_S	$V_S = V_{SA}$		18	27	mA
		input A, C, D: $V_I = 0$ V				
Power consumption	P	input B: $V_I = V_{SA}$		270	460	mW

Delay times, $V_S = 15$ V, $T_A = 25$ °C

Propagation delay						
from B to dec 2	t_{PLH}	$V_{SC} = 12$ v				ns
	t_{PHL}	$R_C = 1$ kΩ				ns
from B to dec 0	t_{PLH}	$C_L = 10$ pF				ns
	t_{PHL}					ns

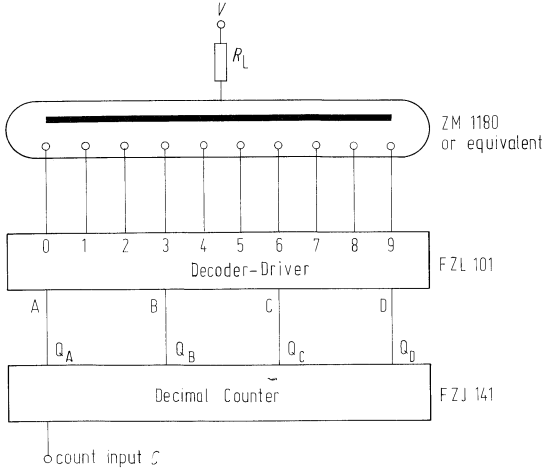


Pin configuration, top view

Truth table

BCD-inputs D	C	B	A	decimal outputs 0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

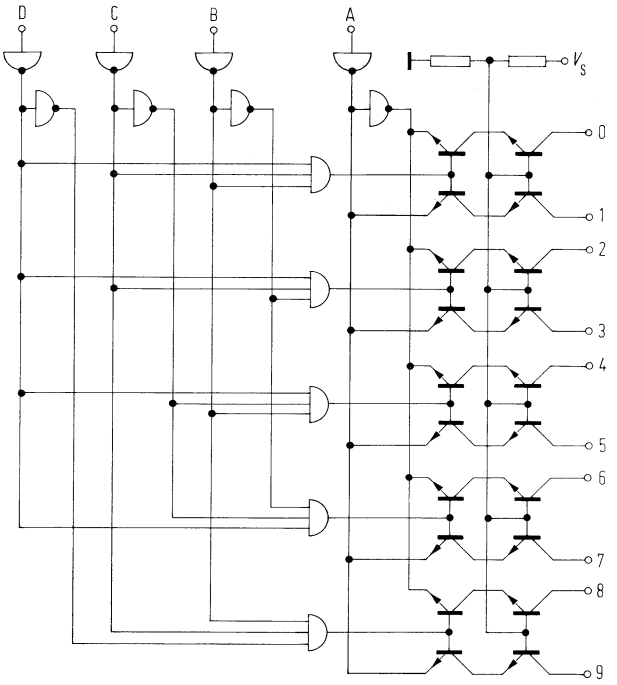
Application with indicator tube



Notes:
Recommended supply voltage for the indicator tube $V_S = 200$ V
Resistance R_L depends on the lighting voltage V_B and the lighting current I_B of the indicator tube.
as follows:

$$R_L = \frac{V - V_B}{I_B}\ \Omega$$

Block diagram



Type	ordernumbers
FZL 111	Q 67000–L 156
FZL 115	Q 67000–L 161

The FZL 111/115 transform BCD-words with 4 bits present at the inputs A, B, C, D into the 7-segment code. Control functions are provided by means of three auxiliary inputs, BI, RBI, LT. An L-signal at the ripple-blanking-input RBI suppresses the decimal O-signal at the outputs. The ripple-blanking-output RBQ (internally connected with BI) provides an automatic O-suppression over several decades. When the blanking input BI is supplied with an L-signal, all outputs are blocked. An L-signal at the lamp-test-input LT forces all outputs into conduction. In addition the following maximum ratings apply:

Maximum ratings

		test condition	lower limit B	upper limit A	unit
Output voltage for the outputs a to g	V_Q	T_Q blocked	0	16.5	V
Output current	I_Q	T_Q blocked	0	25	µA
Output current for the outputs a to g	I_{QL}	T_Q conducting	0	20	mA
outputs a to g, duty cycle 1:1	I_{QL}	T_Q conducting	0	40	mA

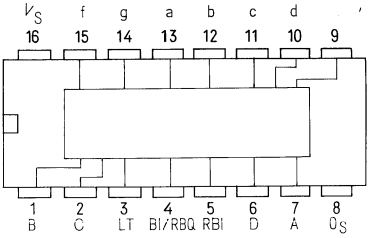
Electrical characteristics
12-V-range
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-output voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
L-output voltage for the outputs a to g	V_{QL}	$I_{QL}=20$ mA		0.4	0.7	V
	V_{QL}	$I_{QL}=40$ mA $V_S=V_{SB}$		0.7	1.0	V
Output BI/RBQ	V_{QL}	$I_{QL}=7.5$ mA			1.7	V
Output voltage for the outputs a to g	V_Q	$V_S=V_{SB}$, $I_Q=25$ µA			16.5	V
H-output voltage at BI/RBQ	V_{QH}	$V_S=V_{SA}$, $-I_{QH}=0.1$ mA	10.0	11.3		V
DC-noise margin						
H-signal	V_{nm}		2.5	5.0		V
L-signal	V_{nm}		2.8	5.0		V
H-input current						
at A, B, C, D, RBI	V_{IH}				10	µA
at BI/RBQ	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$			20	µA
at LT	I_{IH}				30	µA
L-input current						
at A, B, C, D, RBI	I_{IL}			1.0	2.1	mA
at BI/RBQ	I_{IL}	V_SV_{SA}, $V_{IL}=1.7$ V		2.0	4.2	mA
at LT	I_{IL}			3.0	5.3	mA
supply current	I_S	$V_S=V_{SA}$, outputs open			40	mA

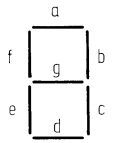
Electrical characteristics

15-V-range
temperature ranges 1 and 5

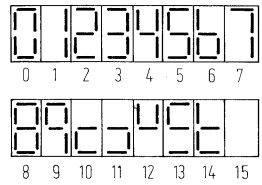
		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		13.5	15.0	16.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-onput voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
L-output voltage for the						
outputs a to g	V_{QL}	$I_{QL}=20$ mA		0.4	0.7	V
	V_{QL}	$I_{QL}=40$ mA $V_S=V_{SB}$		0.7	1.0	V
Output BI/RBQ	V_{QL}	$I_{QL}=9$ mA			1.7	V
Output voltage for the						
outputs a to g	V_Q	$V_S=V_{SB}$, $I_Q=25\,\mu$A			16.5	V
H-output voltage at BI/RBQ	V_{QH}	$V_S=V_{SA}$, $-I_{QH}=0.1$ mA	12.0	14.3		V
DC-noise margin						
H-signal	V_{nm}		4.5	8.0		V
L-signal	V_{nm}		2.8	5.0		V
H-input current						
at A, B, C, D, RBI	V_{IH}				10	μA
at BI/RBQ	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$			20	μA
at LT	I_{IH}				30	μA
L-input current						
at A, B, C, D, RBI	I_{IL}				2.6	mA
at BI/RBQ	I_{IL}	$V_S V_{SA}$, $V_{IL}=1.7$ V			5.2	mA
at LT	I_{IL}				7.8	mA
supply current	I_S	$V_S=V_{SA}$, outputs open			44	mA



Pin configuration
top view



Segment
identification



Output
patterns

Truth table

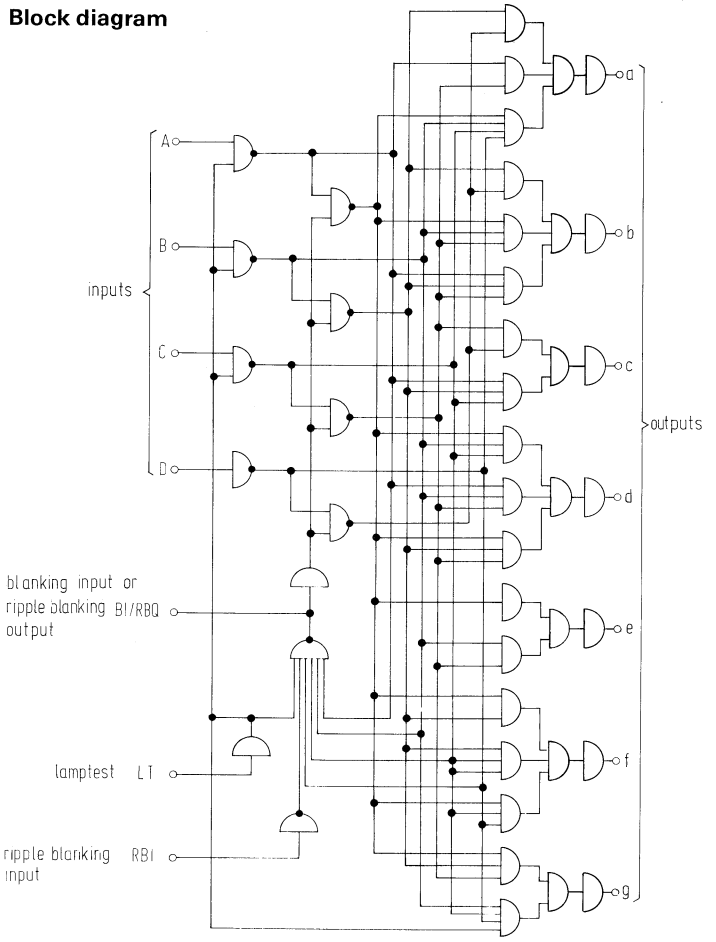
function	LT	RBI	D	C	B	A	BI/RBQ	a	b	c	d	e	f	g
0[1]	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H
BI[2]	X	X	X	X	X	X	L	H	H	H	H	H	H	H
RBI[3]	H	L	L	L	L	L	L	H	H	H	H	H	H	H
LT[4]	I	x	x	x	x	x	H	L	L	L	L	L	L	L

Notes:

X = H or L-signal

1) IF O-indication is disired, RBI must be supplied with an H-signal.
2) An L-signal at BI forces all segment outputs into H-state independent of the other input conditions.
3) If an L-signal is supplied to RBI and A, B, C, D, H-signals result at all outputs and L-signal at RBQ (zerocondition).
4) An L-signal at LT switches all outputs to L only if BI/RBQ is supplied with an H-signal regardless of the input condition at A, B, C, D, and RBI.

Block diagram



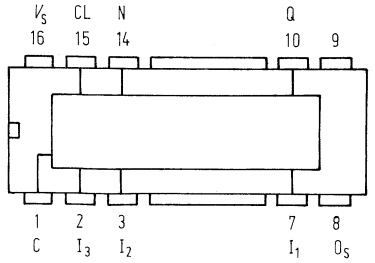
Tentative Data

Type	order numbers
FZL 121	Q 67000–L 168

The FZL 121 is a power stage for output currents up to 400 mA. The FZL 121 has 3 NOR gate inputs with Schmitt Trigger characteristics. The load is connected between the output Q (open collector) and V_S. If a short circuit occurs the current is turned off. The circuit checks periodically whether the short circuit is still present.

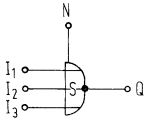
Electrical characteristics
temperature range 1

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	15.0	20	V
H-input voltage	V_{IH}		8			V
L-input voltage	V_{IL}				6	
Hysteresis	V_H			0.4		V
L-output voltage	V_{QL}	$V_I=V_S$; I_Q=0,4 A		1,6	2.6	
Input current	I_I	2 V<V_I<V_S	0.1		0.2	mA
Output current	I_Q				400	mA
Supply current	I_S	I_Q=0		5		mA
Capacitance at CI	C_{CI}	clock frequency 0,5 kHz		39		nF
Capacitance at N	C_{N1}			500		pF
	C_{N2}			1.8		nF
Nominal lamp current	I_Q				150	mA
Capacitive loads	C_L				each C_N	nF

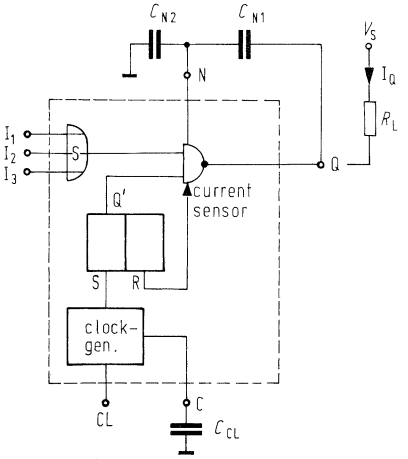


Pin configuration
top view
inputs: I_1, I_2, I_3
output: Q
pins 4 to 6 and 11 to 13 are connected
to provide a heat sink

Logic diagram for normal operation



Logic diagram for short-circuit operation



To avoid oscillations during a short circuit it is necessary to connect two capacitors to the N-terminal (C_{N1}, C_{N2}). By means of C_{N1} the transition at the output Q can be varied.
A capacitor C_{CI} between the C-terminal and ground is required for the clock generator. Up to 8 clock terminals CI of the types FZL 121, FZL 131 may be combined in parallel so that only one capacitor C_{CI} is required. The C-terminals of the remaining circuits must be connected to V_S.
Inductive loads must be provided with a quench diode.

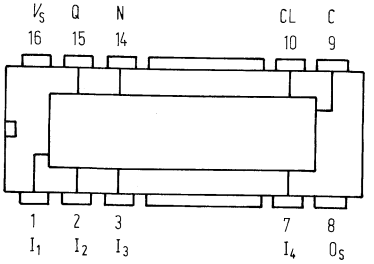
Tentative Data

Type	order numbers
FZL 131	Q 67000–L 169

The FZL 131 is a power stage for output currents up to 400 mA and for nominal lamp currents of up to 150 mA. The FZL 131 has four OR gate inputs with Schmitt Trigger characteristics. The load is connected between the output Q (open emitter) and O_S. If a short circuit occurs the current is turned off. The circuit checks periodically whether the short circuit is still present.

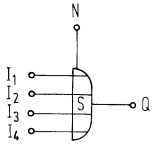
Electrical characteristics
temperature range 1

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	15.0	20	V
H-input voltage	V_{IH}		8			V
L-input voltage	V_{IL}				6	V
Hysteresis	V_H			0.4		V
H-output voltage	V_{QH}	$-I_Q$=0.4 A	V_S−3 V	V_S−1.8V		V
Input current	I_I	2 V <V_I<V_S	0.1		0.2	mA
Output current	$-I_{QH}$				400	mA
Supply current	I_S	I_Q=0		5		mA
Capacitance at CI	C_{CI}			39		pF
Capacitance at N	C_{N1}			500		pF
	C_{N2}			1.8		nF
Nominal lamp current	I_Q				150	mA

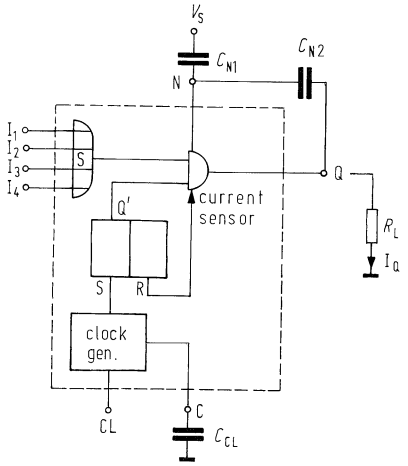


Pin configuration
top view
inputs: I_1, I_2, I_3, I_4
output: Q
pins 4 to 6 and 11 to 13 are connected to provide a heat sink

Logic diagram for normal operation



Logic diagram for short-circuit operation



To avoid oscillations during a short circuit it is necessary to connect two capacitors to the N-terminal (C_{N1}, C_{N2}). By means of C_{N1} the transition time at the output Q can be varied.
A capacitor C_{CI} between the C-terminal and ground is required for the clock generator. Up to 8 clock terminals CI of the types FZL 121, FZL 131 may be combined in parallel so that only capacitor C_{CI} is required. The C-terminals of the remaining circuits must be connected to V_S.
Inductive loads must be provided with a quench diode.

Tentative Data

Type	order numbers
FZL 141	Q 67000–L 170

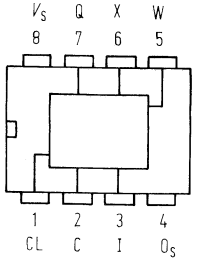
The FZL 141 is a driver for transistor power stages with output currents up to 3 A. The output of the controlled power stage is short-circuit proof. If a short circuit occurs the current is turned off. The circuit checks periodically whether the short circuit is still present. The load is connected between the output Q_1 (i. e. Q_2 of the power stage) and O_S. The FZL 141 has a Schmitt Trigger input.

Electrical characteristics
temperature range 1

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	15.0	20	V
H-input voltage	V_{IH}		8			V
L-input voltage	V_{IL}				6	V
Hysteresis	V_H			0.4		V
Input current	I_I	$2\,V<V_I<V_S$	0.1		0.2	mA
Output voltage	V_{Q1}	I_{Q1}=0.5 A with BD 138	V_S–1.8V	V_S–1 V		V
Output voltage	V_{Q2}	I_{Q2}=3 A with BCW 76, 2N3055	V_S–3.2V	V_S–2V		V
Turn off voltage for overload	V_W			V_S–0.8V		V
Input current at X	I_X				25	mA
Output current at Q	$-I_Q$				25	mA
Output current at Q_1	I_{Q1}	R_K=1.6Ω BD 138			500	mA
Output current at Q_2	I_{Q2}	R_K=0.33Ω, BCW 76 2N3055			3	A
Resistance	R_V		$\frac{V_S-1\,V}{I_Q\,mA}$			kΩ

Recommended transistors for the following amplifier stage:

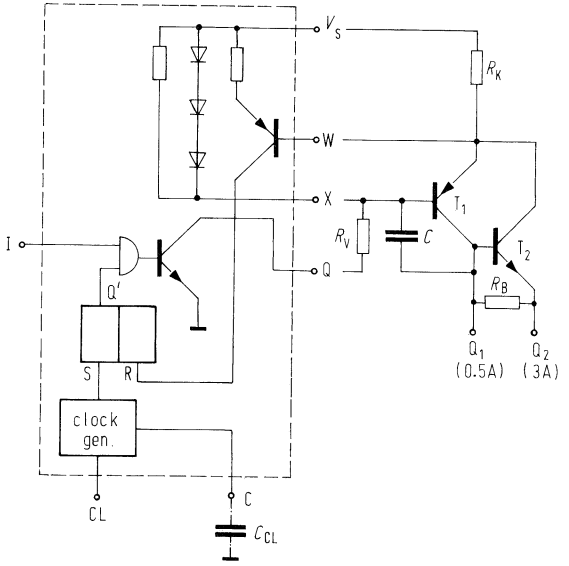
Use of one stage (output current 0.5 A) : T_1 = BD 138–10
Operation of two stages (output current 3 A) : T_1 = BCW 76–16,
T_2 = 2N3055



Pin configuration
top view
Input: I
input for short circuit protection: W, X
output: Q

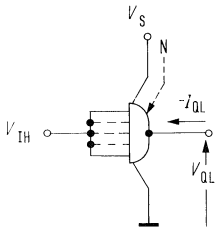
Logic diagram for normal operation

Logic diagram for short-circuit operation

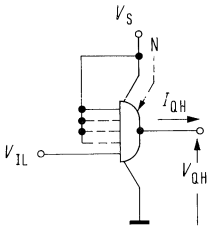


To avoid oscillations short circuit during it is necessary to connect a capacitor between the base and collector of transistor T 1. A capacitor C_{CI} between the C-terminal and ground is required for the clock generator. Up to 8 clock terminals CI of the types FZL 121, FZL 131, FZL 141 may be combined in parallel so that only one capacitor C_{CI} is required. The C-terminals of the remaining circuits must be connected to V_S.

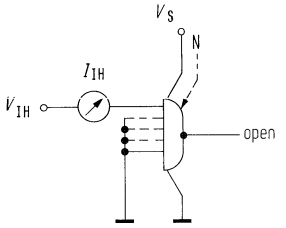
The test circuits are shown for NAND-gates. They apply similarly for gates with other functions.



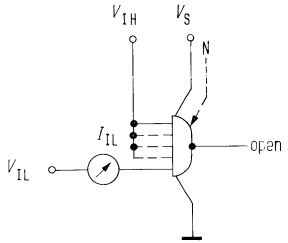
test circuit 1



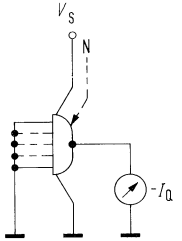
test circuit 2



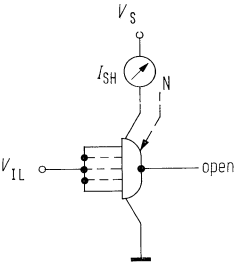
test circuit 3



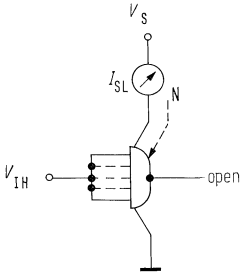
test circuit 4



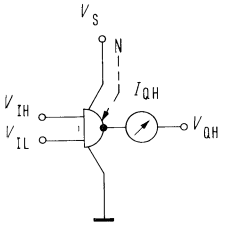
test circuit 5



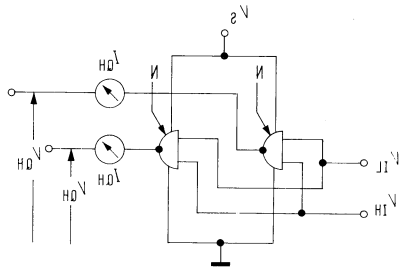
test circuit 6



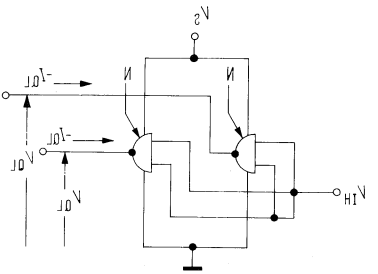
test circuit 7



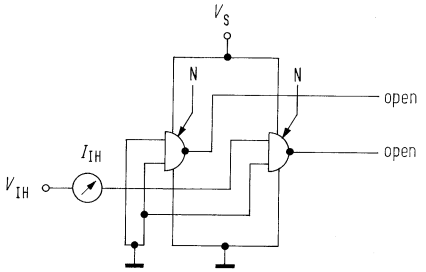
test circuit 8



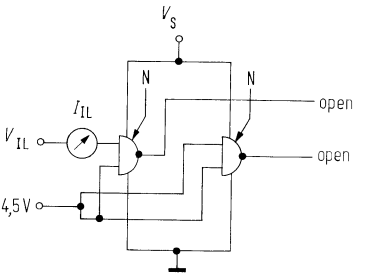
test circuit 9



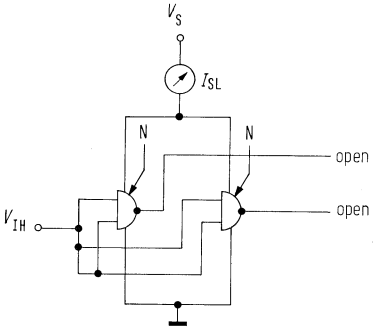
test circuit 10



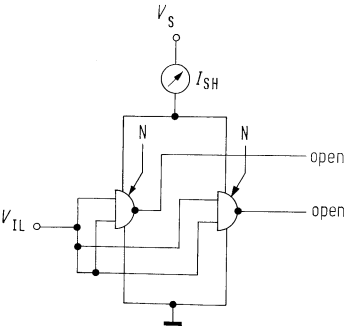
test circuit 11



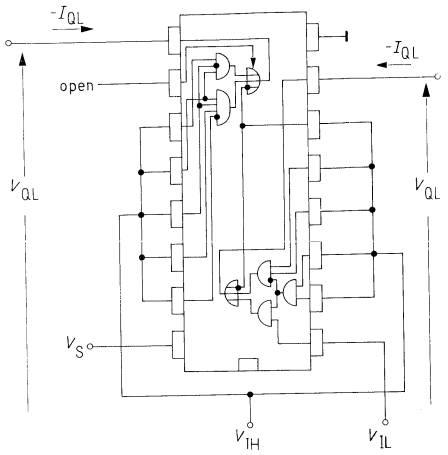
test circuit 12



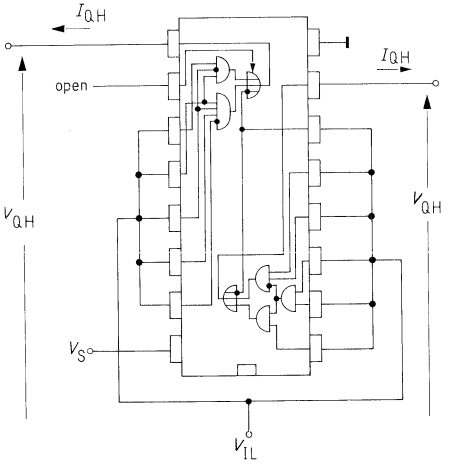
test circuit 13



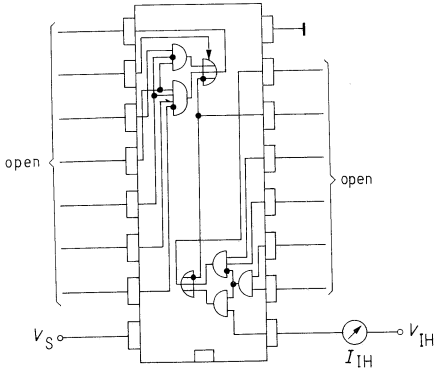
test circuit 14



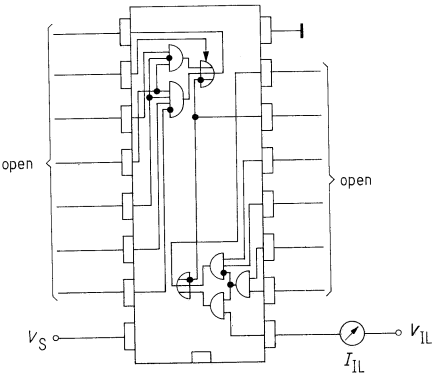
test circuit 15



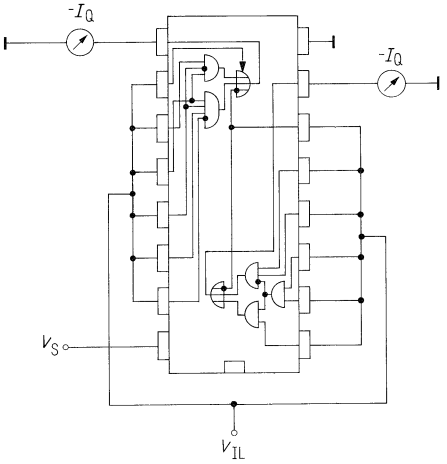
test circuit 16



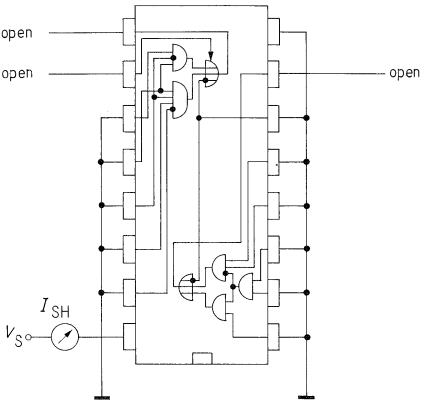
test circuit 17



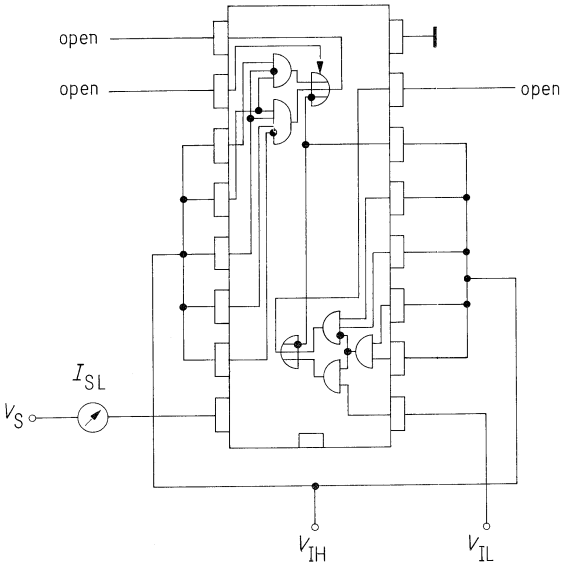
test circuit 18



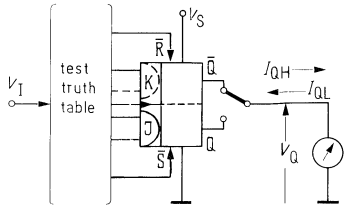
test circuit 19
each output in tested seperately



test circuit 20

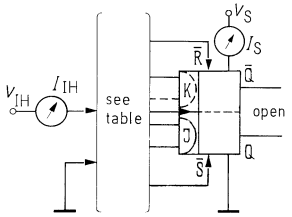


test circuit 21



test circuit 22

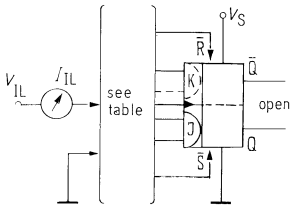
each output is tested seperately



test circuit 23

I_{IH}: each input is tested seperately
I_S: V_{IH} is applied to all inputs

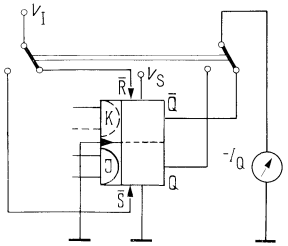
V_{IH} at	ground at
J_1 or J_2	T, $\overline{S}$, J_1, or J_2
K_1 or K_2	T, R, K_1, or K_2
$\overline{R}$	T, J_1, and J_2
$\overline{S}$	T, K_1, and K_2
T	J, J, K, K, $\overline{R}$, S



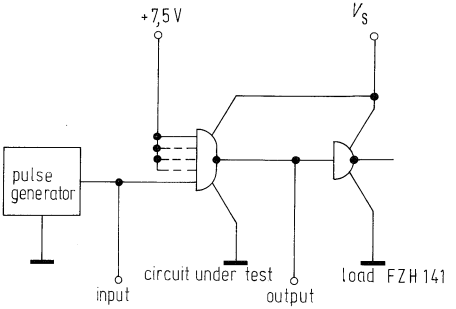
test circuit 24

each input is tested seperately

V_{IL} at	4.5 V at	17 V at
J_1, or J_2	$\overline{R}$	T, J_1, or J_2
K_1, or K_2	$\overline{S}$	T, K_1, or K_2
$\overline{R}$		J_1 and J_2
$\overline{S}$		K_1 and K_2
T		J_1, J_2, K_1, K_2

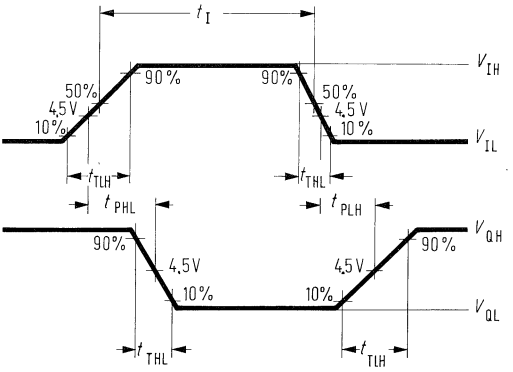


test circuit 25

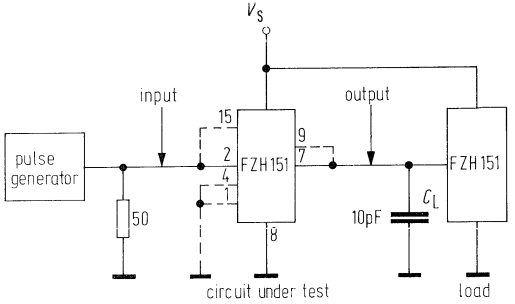


test circuit 26

pulse diagram

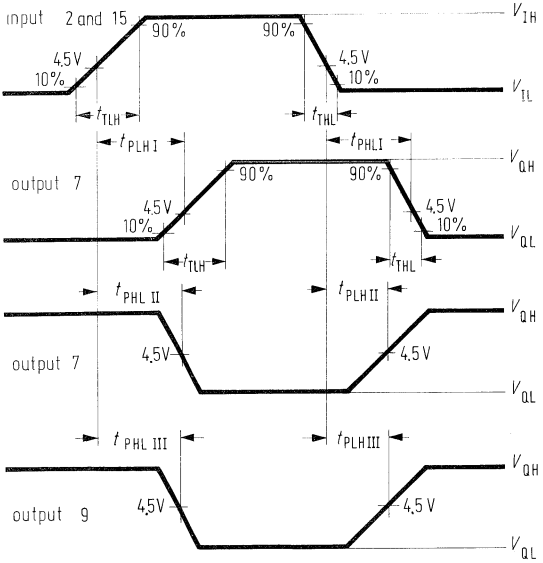


Notes:
generator: t_{TLH} = 350 ns, t_{THL} = 120 ns, t_p = 1 µs, amplitude: +10 V.
the load consits of stray and jig capacitance and one gate FZH 141.



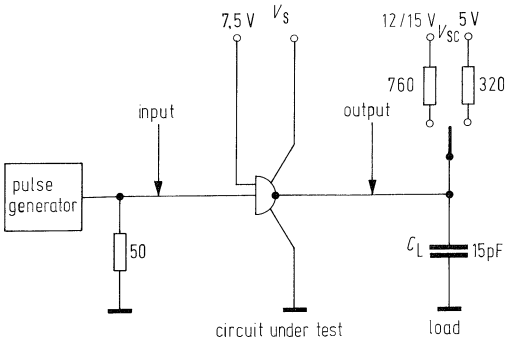
test circuit 27

pulse diagram



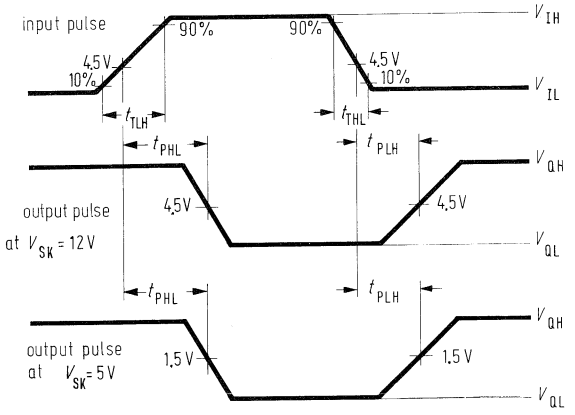
Notes:
generator: t_{TLH} = 350 ns, t_{THL} = 240 ns; amplitude: +10 V.

When measuring t_p between input 2 and output 7, two tests must be made. During the first test input 4 must be grounded. During the second test input 1 must be grounded. When measuring t_p between input 15 and output 9, all inputs must remain open. t_{TLH} and t_{THL} are measured at output 7.

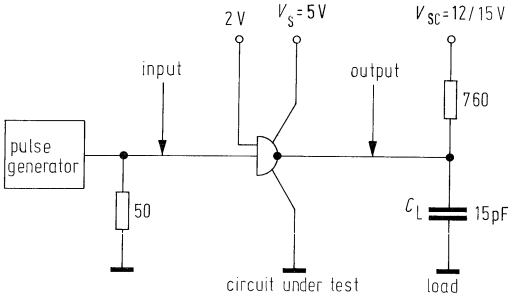


test circuit 28

pulse diagram

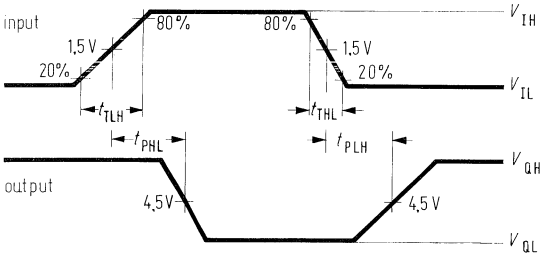


Notes:
generator: t_{TLH} = 350 ns, t_{THL} = 120 ns; amplitude: +10 V.
levels: input pulse 4.5 V above ground, output pulse 1.5 V for V_{SC} = 5 V and 4.5 V for V_{SC}=12 V above ground.

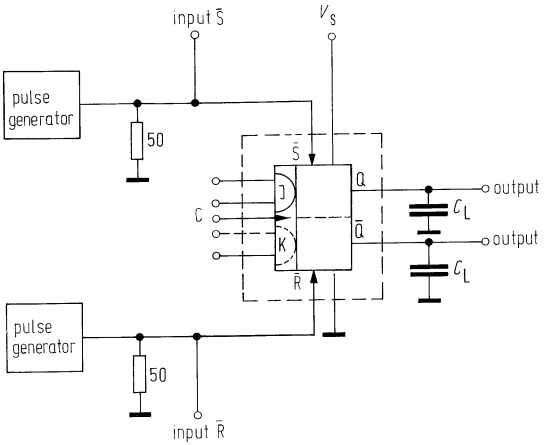


test circuit 29

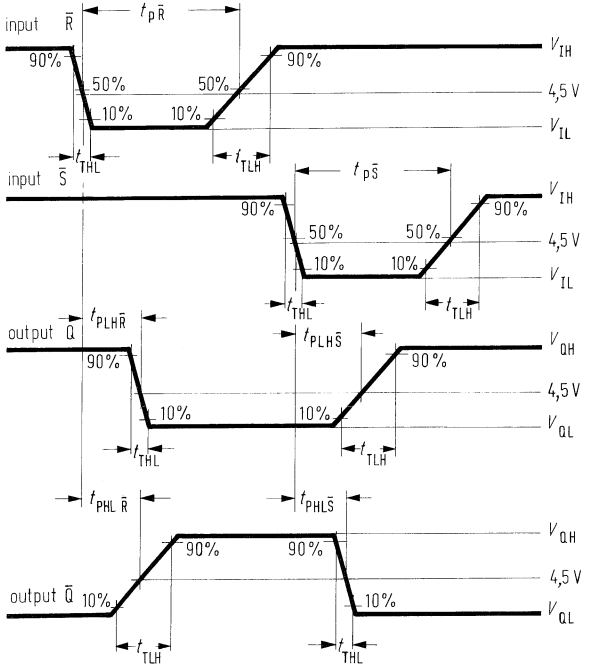
pulse diagram



Notes:
generator: t_{TLH} = 10 ns, t_{THL} = 5 ns; amplitude: +3 V.
levels: input pulse 1.5 V above ground, output pulse 4.5 V above ground.

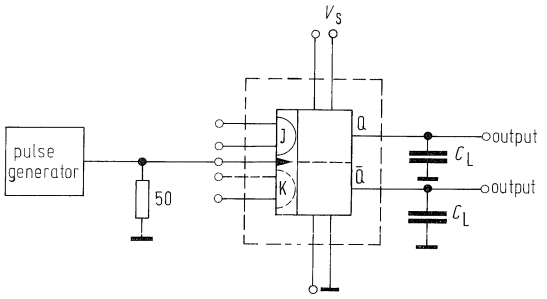


test circuit 30



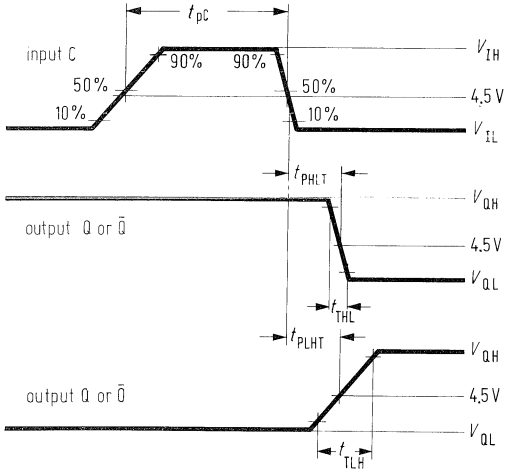
pulse diagram

Notes:
generator: t_{THL} = 350 ns,
t_{TLH} = 120 ns,
$t_{pR} = t_{pS}$ = 700 ns
amplitude: +10 V
unused
inputs remain open C_L includes jig and stray capacitance
$t_{PHL\bar{R}}$ and $t_{PLH\bar{S}}$ are referred to 4.5 V above ground.

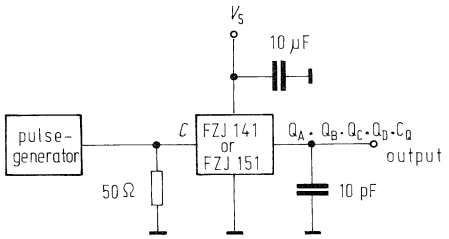


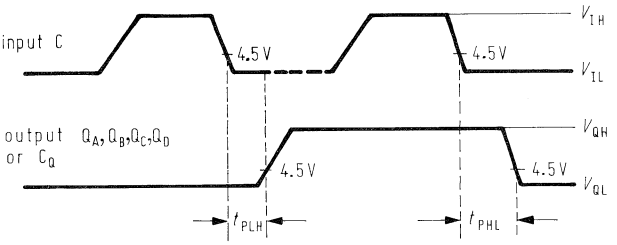
test circuit 31

pulse diagram

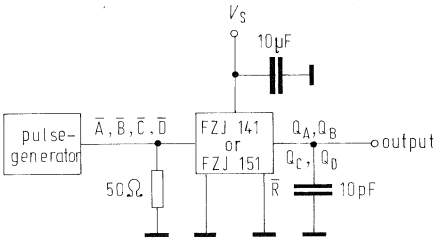


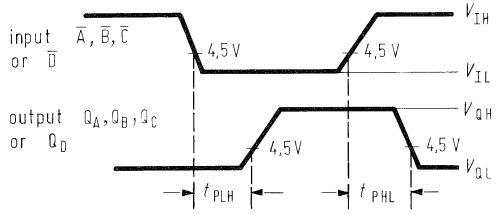
Notes:
generator: t_{TLH} = 350 ns, t_{THL} = 120 ns, t_{pT} = 400 ns
amplitude = +9 V, +1 V offset
unused inputs remain open
C_L includes jig and stray capaditance.
t_{PHLT} and t_{PLHT} are referred to 4.5 V above ground.



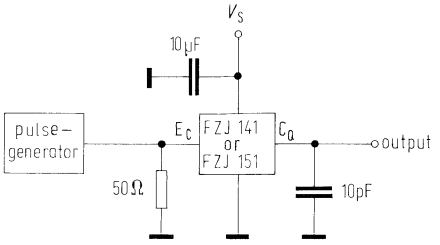


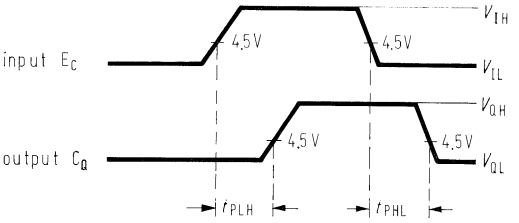
test circuit 50
connect unused inputs to V_S





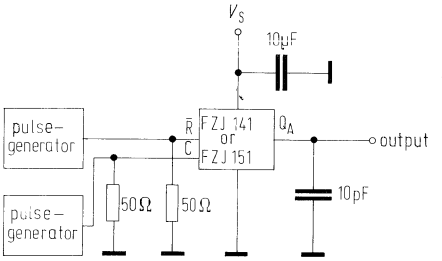
test circuit 51
connect unused inputs to V_S

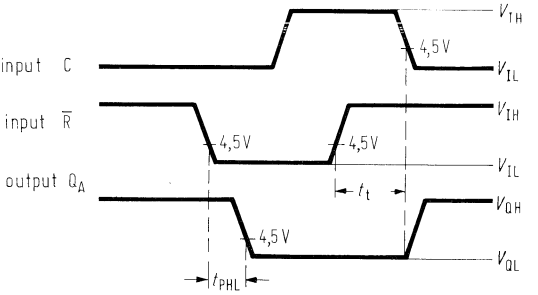




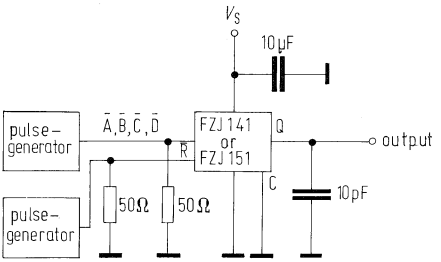
	inputs $\overline{A}$	$\overline{B}$	$\overline{C}$	$\overline{D}$	$\overline{R}$	C	output C_Q
FZJ 141/5	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{QH}
FZJ 151/5	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{QH}

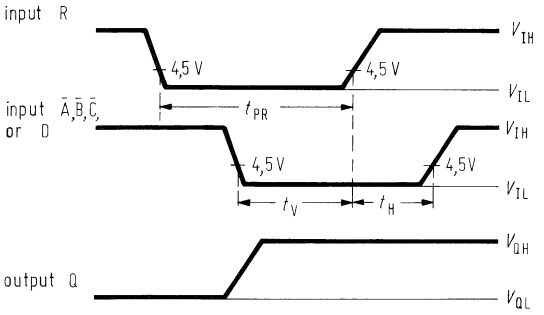
test circuit 52





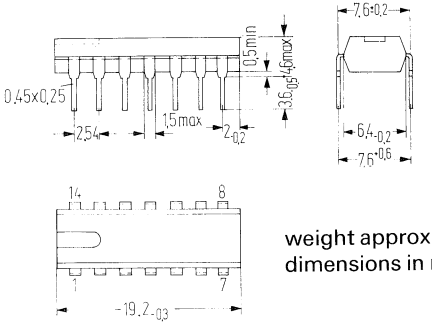
test circuit 53
connect usued inputs to V_S





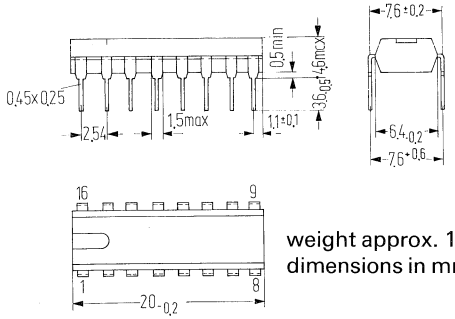
test circuit 54
connect unused inputs to V_S

Plastic dual-in-linie package 14 pins 20 A 14 DIN 41 866 (TO-116)



weight approx. 1.1 g
dimensions in mm

Plastic dual-in-line package 16 pins 20 A 16 DIN 41 866



weight approx. 1.2 g
dimensions in mm

Application Notes

5. Application Notes

The slow, noise-immune logic-series FZ 100 is designed for all applications that require high static and dynamic noise immunity. For especially critical applications the delay time of the series FZ 100 can be extended by using additional capacitors. In this way the dynamic noise immunity can be adjusted to suit the given conditions. In most cases the addition of capacitors only to the input gates of a system is sufficient. The delay capability is especially important when the transmission line between signal source and receiver is extremely long. The choice of suitable additional capacitors on the receiving gate makes it possible to efficiently suppress external interference.

The requirements on the power supply are not severe. A regulation accuracy from 10 to 15% is sufficient. The internal resistance of the power supply is not critical, because the LSL-components exhibit no switching spikes. On the other hand it is important that the minimum limit of the supply voltage (V_S) in the 12 V range be fixed at 11,4 V and that the maximum limit in the 15 V range is 17 V. Outside these voltage values, the logic function is not guaranteed and the destruction of components can occur for voltages above 18 V.

In LSL circuits crosstalk is practically non-existent. Therefore there are no rules relating to the distances, lengths or layout of the conductors on a printed circuit board.

A selection of various applications examples for the LSL-series FZ 100 will now be considered. Most circuits are shown without supply voltage connections. The recommended supply voltages are $V_S = 12$ V and $V_S = 15$ V.

5.1 System Concepts Using Noise-Immune LSL Elements of the FZ 100 Series

In digital control systems, noise immunity is a factor of the greatest importance. The technical features of the FZ 100 series of noise-immune low-speed logic elements allow far more favorable circuit design than other types of logic. The features of importance in connection with the noise immunity of an LSL system are primarily the voltage supply, the PC board, the wiring frame, the cabinet design and the signal transmission path.

Unlike with mechanical systems, it is necessary in designing electronic digital control systems to proceed from the assumption that their functioning is liable to be impaired by noise voltages. Such voltages may be either pulses produced, say, as the result of an unfavorable interconnection pattern, or may be picked up from outside the system, whereby the extent of the external noise voltages at the site of the system is often unknown, and the problems first arise after the system has been commissioned. The system should therefore be so designed that noise voltages will be intercepted before reaching the logic assembly. Noise suppression at the input is here of particular importance. Our LSL series offers a large degree of freedom in this respect by allowing the addition of noise suppression capacitors. Provision is made for these capacitors at the planning stage and, if necessary, they can be adapted to the existing conditions on site. Guidelines for practical system design will be given in the following.

Power Supply

The use of separate power supplies and leads for feeding the various parts of the system offers the optimum solution. This sectionalization precludes the possibility of noise interfering with other parts of the systems for example when a rise in current in the power section causes voltage drops across a common reference lead.

Effective immunity to RF noise superimposed on the line ac voltage is provided by a primary side line voltage filter. Although such filters are not always necessary, they reduce the danger of malfunctions. The B81931A... series is among the suitable types.

Large fluctuations in line voltage and load current can only be compensated with a voltage regulator. To minimize the effect of changes in load current, the internal resistance R_i should be less than $1\,\Omega$.

Provided that the load current of the LSL system does not vary during operation by more than a certain extent, a power section consisting of a transformer, a bridge rectifier and a charging capacitor will be sufficient. For example:

The functioning of LSL systems is assured over a supply voltage range V_S of 11.4 to 17 V; the AND-OR gate FZH 151 still functions at a voltage V_S of 10.5 V. Optimum utilization of this voltage range is possible by choosing a supply voltage of intermediate value, i.e. 14.5 V. The commonly permissible line ac voltage fluctuation is −15% and +10%. Referenced to V_S=14.5 V, a lower supply voltage of 12.3 V and an upper value of 16 V result. This leaves a margin of ΔV 1 V from the associated limit which can be used as a voltage drop in the case of changes in the load current ΔI. If ΔI is known, the required dynamic internal resistance R_i of the power supply calculates at $\Delta V{:}\Delta I$. In the case of an unregulated supply, the resistance R_i depends largely on the chosen transformer. For switching operations the changes in load current are of the order of microseconds. The reduction of the internal resistance by the charging capacitor is still assured at this speed. Empirical values for the internal resistance of power packs are, for instance, $R_i \approx 5\,\Omega$ for a transformer core M65 with a bridge rectifier

rated for 14.5 V and 1 A. The permissible change in load current is in this case

$$\Delta I = \frac{\Delta V}{R_i} = \frac{\pm 1\,V}{5\,\Omega} = \pm 0.2\,A.$$

Typical guideline values for the change in load current ΔI relative to the average operating current I are 20 to 30%. If a safety margin of 10% is allowed for, the permissible current values are 500 to 700 mA. A power pack such as this is suitable for the operation of 300 gates, 50 flipflops or a corresponding combination of both. The charging capacitor should have a capacitance of about 2 to 3 mF. A 1 nF ceramic capacitor should be connected in shunt with the charging capacitor for suppressing RF noise pulses. If the M65 core is replaced by an M85A core and all other conditions are the same, the stated values will be doubled.
Circuits with the FZH 241 Schmitt trigger need, if an unregulated power supply is used, a 1 µF capacitor, which should be mounted as close to the terminals of the package as possible.

PC Board

LSL elements do not produce any undesired signal crosstalk. The length, spacing and layout of the signal transmission leads on the PC board can therefore be chosen arbitrarily. To assure the positive avoidance of coupling noise and mode excitation, the leads to the N terminals of LSL elements must not be longer than 5 cm. Links between the function inputs of the FZK 101 timing circuit must not be longer than 5 mm and the leads to its RC terminals should be kept as short as possible.
The layout of the leads to points V_S and O_S is not critical if only LSL elements have to be fed. A capacitor with a capacitance $C \geqq 10\,\mu F$ will improve the protection of the standard European PC board from short-term voltage dips. If additional load currents from relays and lamps mounted on the same board flow through the supply leads, a common ground plane with a mesh structure will be necessary. Owing to its favorable constructional design and low cost, the use of this system is generally recommendable.

Rack Wiring

Owing to the high permissible mutual capacitance of two signal transmission lines, LSL elements allow flexibility in wiring routes. Only long leads with an unfavorable path may have to be protected by choosing elements with a wired N terminal. For further details please refer to the section on signal transmission and noise immunity. A rack power supply lead-network of low impedance with thick ground wires or ground plates will reduce the danger of external noise pickup.

Cabinet Design

In the cabinet the signal transmission lines must be protected according to their length and location as described in the next section. These measures are particularly important if the cabinet also accommodates thyristors, triacs, motors, relays, contactors and other sources of serious RF noise. A ground bar is required for ground potential. All ground and RF shielding leads must be connected to the ground bar by short low-impedance leads. Line voltage leads in the cabinet, as well as the input and output leads of the power and control sections, must be RF shielded. The control electronics must be isolated from the case to avoid noise pickup.

Signal Transmission and Noise Immunity

The following also applies to the cabinet design, the rack wiring and the LSL transmission lines.

Since the possible length of a signal transmission line is limited by the noise level and the associated changes in potential, it is always advantageous to choose shielded cables with twisted pairs for all transmission lines of over 10 m in length. Undesired electromagnetic effects are in this case largely suppressed. Twisted signal transmission and ground wires provide increased protection from strong RF interference fields.

For n mutually interfering gates without a wired N-terminal, the following transmission line lengths l have been empirically determined

n = 2 l ~30 m
n = 5 l ~10 m
n = 10 l ~ 5 m

With the N terminal wired, transmission lines of over 100 m length have already been realized

The noise immunity of LSL elements to external noise pickup was tested using a noise simulator. Fluorescent tubes were turned on, contactors operated and differentiating pulses transmitted over one pair of a multicore shielded cable, 20 m long. LSL signals were simultaneously transmitted over another pair of the cable. The insertion of a 1 nF capacitor C_N, was sufficient to provide noise immunity. The appropriate circuit configurations are shown in Fig. 5.1 a, b. The configuration shown in Fig. 5.1 c is suitable for line lengths of over 20 m under conditions of extreme noise. The BAY 60 diodes protect the LSL element from destruction by sharp positive and negative voltage spikes. The dynamic noise immunity is adjustable with capacitor C_N.

The following capacitances are sufficient to suppress noise pulses up to a pulse duration t

t = 10 ms C_N = 1 uF
t = 1 ms C_N = 100 nF
t = 100 µs C_N = 10 nF
t = 10 µs C_N = 1 nF
t = 1 µs C_N = 100 pF.

The permissible noise pulse duration can be lengthened by increasing the capacitance. In practice, however, noise pulses of longer than 5 ms are hardly to be expected. The Schmitt trigger S supplies pulses with an adequately short rise time at subsequent dynamic inputs. Fig. 5.1 d shows the noise immunity behaviour.

Fig. 5.1a

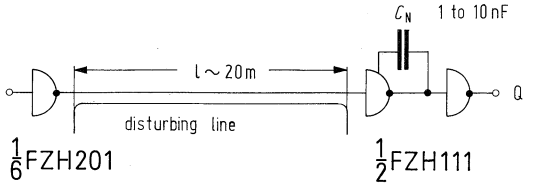


Fig. 5.1b

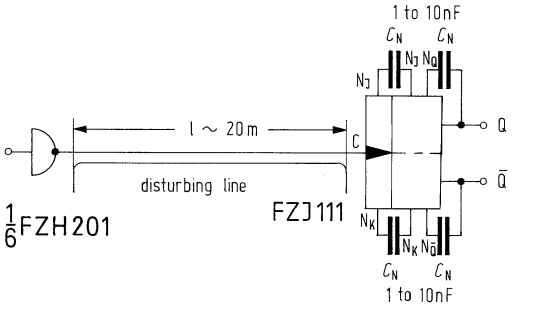


Fig. 5.1c

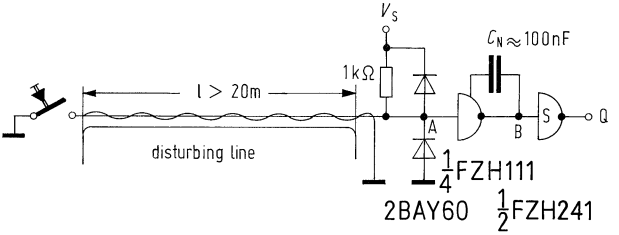


Fig. 5.1d

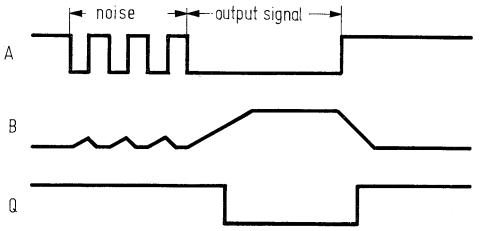
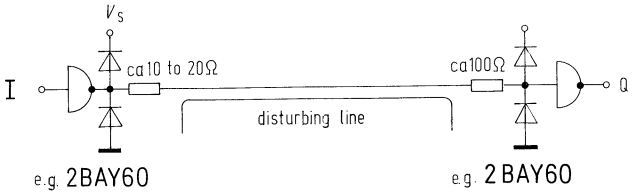


Fig. 5.1e



Storage elements need careful consideration because RF noise at the inputs and also via the supply is liable to produce permanent misinformation. Here again wiring the N-terminal assures effective protection from inductive or capacitive noise. (See also section 5.2) Fig. 5.1b shows a suitable configuration for flipflops. With flipflops, which consist of crosscoupled NAND-gates, the insertion of a capacitor C_N = 1 to 10 nF at one gate is usually sufficient. Logic elements without a wired N-terminal (FZJ 131) and with a permissible N-capacitance of C_N < 500 pf (FZJ 141, FZJ 151, FZJ 161 and FZK 101) can be additionally protected by shunting the terminals V_S and O_S with a capacitor C_N = 10 to 100 nF. The wired N-terminal is further suitable for suppressing contact bounce. C_N should then be chosen between 10 and 100 nF, depending on the bounce frequency.

As a general rule it may be said that the unassigned inputs of simple gates and flipflops may be left open. Since the functioning of counters, shift registers and other elements with a higher scale of integration is only assured at a definite input potential, inputs not required in operation should be connected via a protective resistor R = 1 kΩ to the supply voltage. Input lines which are temporarily opened by, say, a relay contact, should always be avoided as being a too frequent source of noise. The remedy is to interpose a resistor R = 1 kΩ between logic elements and the supply voltage V_S. (Fig. 5.1c)

Proposal for System Configuration

Fig. 5.1 shows a digital machine control system configuration consisting of separate sections for signal generation, control logic, power interface, power section, and voltage supply. Interference to the flow of signals is to be expected along the transmission paths between signal generation and control logic as well as at the control logic and power interface. Since noise in the input lines is particularly critical when storage devices follow, the primary function of the control logic is to separate the output signals from the noise. LSL elements here offer an extremely economic solution because they allow the addition of capacitors of any size. If the noise is filtered out, the N-terminal of the logic section need not be wired unless other noise sources are present (as shown in Fig. 5.1). Control logic sections with transmission lines over 100 m in length have already been realized by this means. The choice of a capacitor of appropriate size is here decisive. A useful guideline value for such transmission lines is $C_N > 100$ nF.

The transmission of clock signals over a long line is basically possible as described in the previous section. Since however there is a serious risk of misinformation, the line length should be limited to 20 m. Once again the choice of a capacitor of appropriate size is decisive. Favourable values are $C_N = 1$ to 10 nF.

There is no danger of RF noise pickup with motors, electromagnets, lamps, heating equipment and other power elements with a large time constant because they react only to static signal changes. Since the power interface section contains no storage elements which could produce permanent misinformation, the protection of this transmission path from noise by wiring the N terminal is unnecessary. Although short noise pulses pass through the gates, the power elements do not respond to them. The length of the transmission path is relatively uncritical.

If extreme voltage spikes appear it is further necessary to protect the LSL inputs from destruction. The amount of energy permissible at the input or output without danger of destruction is here typically 1 mWs. Fig. 5.1 e shows a suitable protective circuit. Noise pickup is removed by way of diodes. The series resistors provide adequate current limitation.

The various sections of the system are fed over separate power leads, so avoiding powerline couplings as already noted in the power supply section.

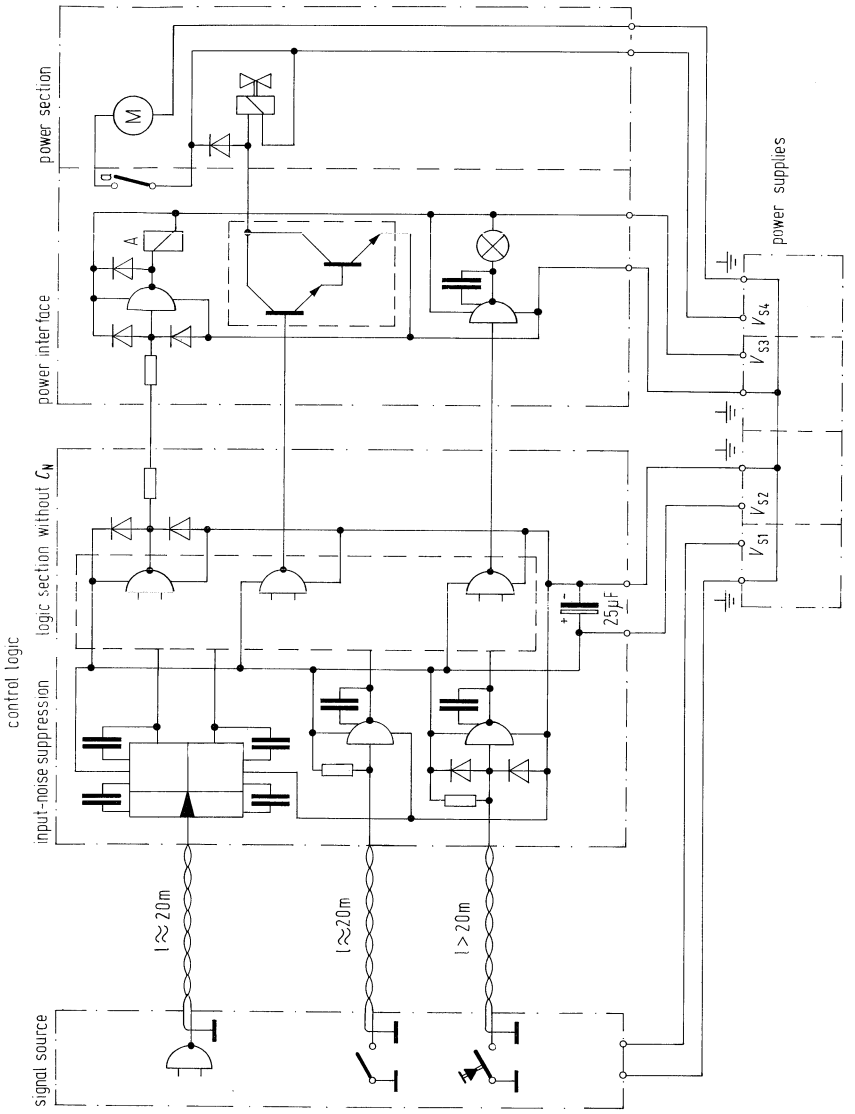

control logic
power section
power interface
logic section without C_N
input-noise suppression
signal source
power supplies
M
A
V_{S1}
V_{S2}
V_{S3}
V_{S4}
25µF
l ≈ 20m
l ≈ 20m
l > 20m

Fig. 5.1

5.2 Noise Immunity and External Components

The noise-immune low speed logic series FZ 100 is favoured for applications requiring a high static as well as dynamic noise immunity. For extremely critical situations, the propagation delay times of the FZ 100-series can be increased by adding capacitors so that the dynamic noise immunity will meet the given conditions. This delaying is especially important in those applications where very long transmission lines are required between the signal source and the receiver. The choice of a suitable capacitor added to the receiving circuit allows the effective suppression of external noise sources. In most cases functional units are protected sufficiently, if the capacitor is added only at the input circiuts.
With gates the capacitor is connected between N-terminal and output Q.
For circuits with mediumscale integration an additional capacitor is connected between the N-node and ground. In this case the effect of noise suppressions at the input is the same as that of a gate.
In comparison, flip-flops FZJ 101 and FZJ 111 require two or four capacitors. Thus three methods of wiring are possible:

a) at the master using a capacitor each between N_J an N_J as well as between N_K and N_K,
b) at the slave with a capacitor each between N_Q and Q as well as between $N_{\overline{Q}}$ and $\overline{Q}$,
c) common at master and slave

In the following table the different wiring modes as well as their advantages are summarized.

Input conditions at			noise voltage at	recommended wiring as described under
T	R or S	J or K		
H	H	X	R or S ↓	b
L	H	X	R or S ↓	a
H	H	X	T ↓	c
L	H	X	T ↑	a
H	H	X	J or K	a
L	H	X	J or K	not required
H	X	X	V_S	not required
L	X	X	V_S	a
X	X	X	Q or $\overline{Q}$	not required

X = L or H
↑ = positive noise voltage
↓ = negative noise voltage

As well as methods a to c a non-symmetrical wiring of master and slave is possible. For approximately the same effect the capacitance has to be 2 to 5 times greater than with symmetrical wiring. In this case however the unequal transition times are disadvantageous.

The table above shows that wiring mode b is suitable for applications of RS-flipflops. The best noise immunity is obtained by mode c. The logic state is maintained at T = L by the slave capacitors and at T = H by the master capacitors. For less critical applications method a is generally sufficient.
The additional capacitors determine the switching times and thus the maximum possible clock frequency. The following values are guidelines:

capacitance C_N [pF]	clock frequency f [kHz]
3000	1
300	10
20	100
0	500

The capacitance C_N is practically unlimited.
Depending on the application of delayed flip-flops, it has to be considered that the following circuits connected to the Q-outputs also operate with delay. This is particularly important if delayed counter circuits are decoded. Overlapping output pulses (spikes) at different decoder outputs are avoidable only if the relevant decoder circuit is also delayed. The recommended ratio of the capacitors at the flip-flop slave C_{NF} to the capacitors at the decoder gate C_N is: $C_{NF} : C_N = 1 : 4$.

5.3 Dynamic Noise Immunity Considerations

The special feature of the LSL-series FZ 100 is the possible addition of capacitors at the N-terminal. This capacitor acts as a Miller integrator and extends the delay times. In this way the dynamic noise immunity can be easily and quickly matched to the requirements of the installation site. In most cases it is sufficient to add delay capacitors only at the input gates of a system as shown in fig. 5.3 a. The control system remains without delay capacitors.
The main task of the input logic is the separation of the noise and the input signals as well as the protection of the system from noise. A slow switching characteristic as shown in fig. 5.3 d is a prerequisite for this task. The active duration of any noise is much shorter than the propagation delay. Any reaction is thus excluded.
The task of the control system is the information processing. The timing of the input signals at I_1 and I_2 determines the required operating speed. In general the system must operate much faster than the input logic.
Interfacing slow input circuits with fast systems can cause problems unless the transition time of the control pulses is sufficiently short. The critical point is the threshold in the vicinity of which the noise immunity is greatly reduced. The probability of an interfering noise pulse is the greater, the slower the threshold is passed. Fig. 5.3 e to f show the possible reaction of various circuits to such noise pulses in the vicinity of the threshold voltage V_S. Fig. d shows a slow input pulse with interfering noise spikes. Fig. e shows that a noise spike during the threshold transition only causes a negligible dip with gates. Any other noise is eliminated. The Schmitt-Trigger does not react to this kind of noise due to different on and off thresholds V_{So} and V_{Su}. Fig. f shows the reaction of circuits such as flipflops, counters and registers. If the input signal shown in fig. d is used as a clock pulse, a noise spike during the transition of the threshold V_S may lead to a premature termination of the clock pulse. If the same conditions happen to exist during the threshold transition at the trailing edge of the input signal, the result will be in the case of a counter 3 increments according to three clock pulses instead of only 1 increment according to one input pulse. Fig. g shows an additional triggering of the timing circuit due to noise spikes at the threshold transition of the trailing edge of the input pulse if the selected output pulse duration t_Q is less than the input pulse duration.
The problems deseribed here apply basically to any system interface. Thus it can be postulated that any interface circuit must also match the transition time adequately. The probability of errors caused by noise is small if the threshold transition is accomplished rapidly. In particular for the LSL-series the following conclusions may be drawn:

1. The additional capacitance C_N must always be of the same value within any system.
2. If circuits with and without capacitance are combined, the capacitance of the interface gate should not be above C_N = 1 to 2 nF. This value is sufficient to suppress noise pulses up to a duration of 10 to 20 µs (fig. 5.3 a).
3. Applications with greater additional capacitances require a pulse former. The Schmitt-Trigger FZH 241 is particularly suited for these cases. Arbitrary capacitances may be applied to circuits in front of the Schmitt-Trigger (fig. 5.3 b).
4. Fig. 5.3 c shows another possibility to eliminate noise by means of additional capacitors. Noise during the threshold transition can pass the 1. stage only. The propagation delay of the 1. stage causes a delay of the threshold transition of the 2. stage so that any such noise is safely eliminated.

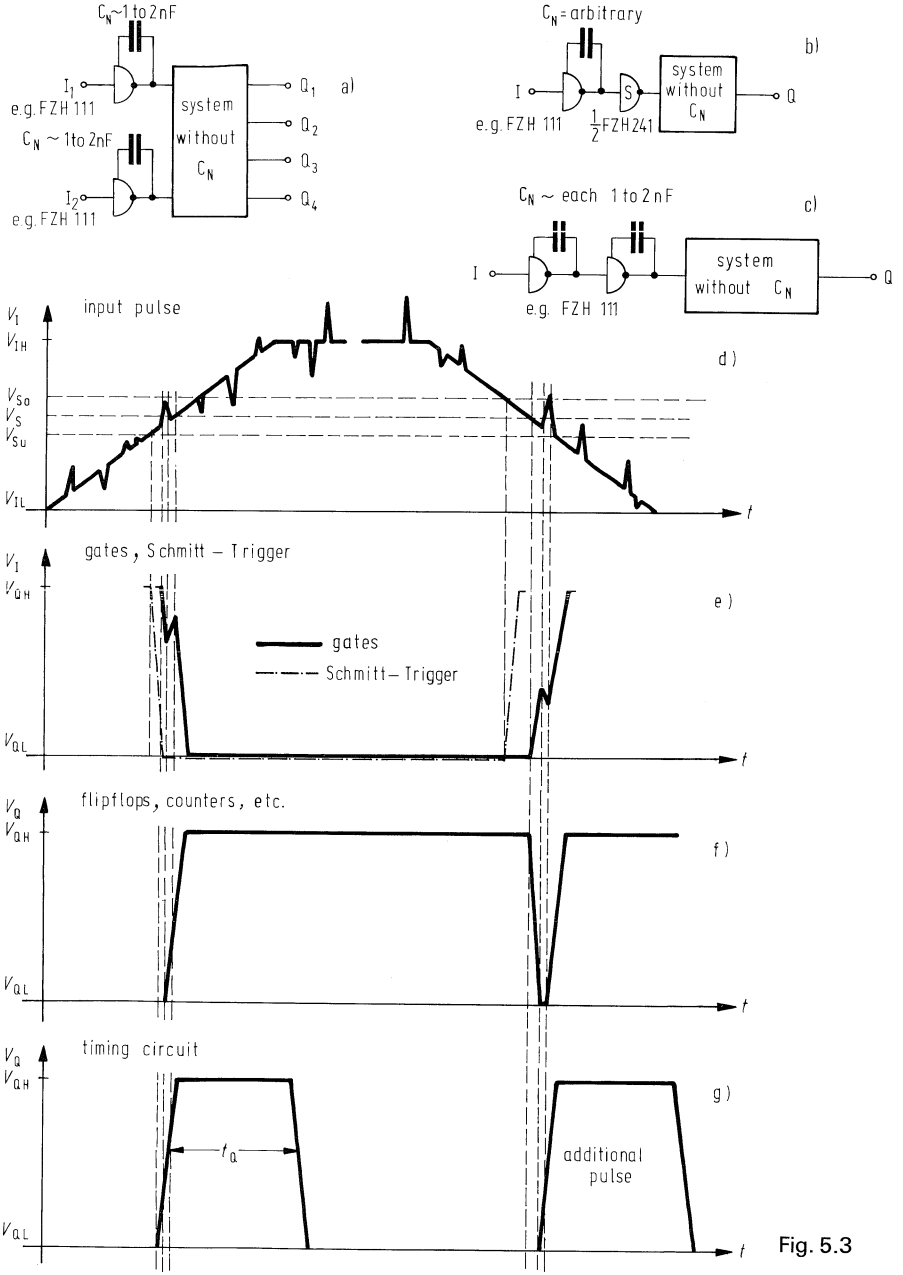

C_N~1 to 2nF
I_1
e.g. FZH 111
C_N ~ 1 to 2nF
I_2
e.g. FZH 111
system without C_N
Q_1
Q_2
Q_3
Q_4
a)
C_N = arbitrary
I
e.g. FZH 111
S
$\frac{1}{2}$FZH241
system without C_N
Q
b)
C_N ~ each 1 to 2nF
I
e.g. FZH 111
system without C_N
Q
c)
input pulse
V_I
V_{IH}
V_{So}
V_S
V_{Su}
V_{IL}
t
d)
gates, Schmitt – Trigger
V_I
V_{QH}
V_{QL}
gates
Schmitt–Trigger
t
e)
flipflops, counters, etc.
V_Q
V_{QH}
V_{QL}
t
f)
timing circuit
V_Q
V_{QH}
V_{QL}
t_Q
additional pulse
t
g)

Fig. 5.3

5.4. Interface Circuits for the LSL-Series FZ 100

The broad application possibilities of the LSL-Series for industrial controls often demand adaptions of the input and output signal levels. The following is a compilation of the most frequently used interface circuits for the LSL-Series FZ 100.

5.4.1 **Circuit to Suppress Contact Bouncing**

Mechanical contacts normally produce bounce frequencies which, depending upon the structure, lie between 10 Hz and 1 kHz. The operating frequencies of digital integrated circuits lie between 500 kHz and 50 MHz. For this reason contact bouncing must be positively avoided if digital circuits are to be mechanically controlled. Otherwise the circuit registers the bouncing as an information change. A simple circuit which supresses contact bouncing is shown in fig. 5.4.1. The cross coupled NAND-gates FZH 101 operate as an RS-flipflop, which is set by the initial key contact. The cross coupling provides a defined input level and therefore a stable output, if the contact bounces.

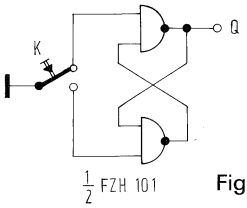
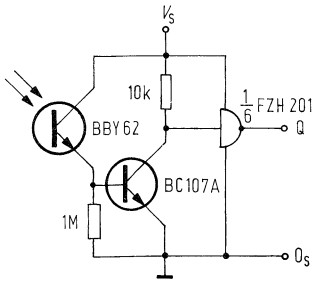


Fig. 5.4.1

5.4.2 **Light Barrier Input**

Light barriers are extensively used in production lines for the piece by piece counting of goods. For the subsequent treatment of the pulses in an LSL-counter, a suitable interface circuit is shown in Fig. 5.4.2. With the aid of a lightbeam the phototransistor BPY 62 drives the following transistor BC 107 A into saturation. The input of the inverter FZH 201 is at an L-potential and the output Q is at an H-level. In the unexposed condition the phototransistor BPY 62 and the transistor BC 107 A are blocked. The inverter input is now at an H-level by means of the resistor 10 kΩ, whilst the output Q is at an L-level. Q is thus in phase with the light barrier pulse. Additional LSL-inputs can be directly connected to the resistor R = 10 kΩ.



5.4.3 **Interfacing with the Optocoupler CNY 17**

Optocouplers offer many important features not feasible with other sensors, for instance chatter free operation, no maintenance, high operating life, electrical separation at insulating voltages of up to 2.5 kV and low noise immunity.
Operation of the optocoupler CNY 17 requires only a few additional components. It is driven by a NAND-gate with open collector, FZH 211. The resistor R = 1 kΩ determines the diode current of I_{ph} ~10 mA at V_S = 12 and of I_{ph} ~13 mA at V_S = 15 V.
Depending on the supply voltages used the collector current of the receiver transistor is I_C = 6 to 8 mA. This ensures a reliable operation of couplers with an efficiency of 60% according to group II. The capacitor of 1 nF is used for noise suppression. This is of great importance when the photodiode is not driven by a LSL-circuit, but by a mechanical contact. Chattering is safely avoided by the choice of a suitable capacitance.
The Schmitt-Trigger provides a sufficiently steep edge for operation of dynamic inputs, e.g. clock inputs of flipflops and counters. The 1 µF capacitor smoothes power supply variations. It is generally required only if unregulated supplies are used. If the transition time of the output pulse is uncritical, the Schmitt-trigger may be replaced by an inverter FZH 201. In this case the 1 µF capacitor is no longer necessary.

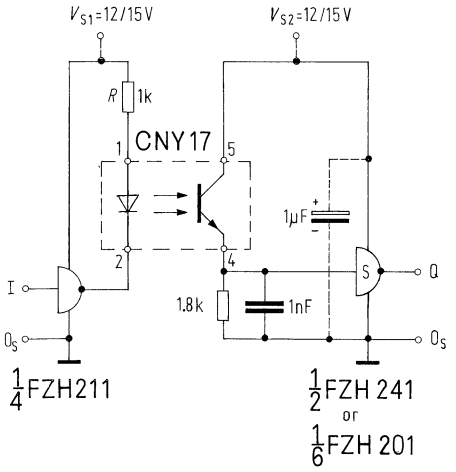


Fig. 5.4.3

5.4.4 **Interface for Negative Input Voltage**

Fig. 5.4.4 shows an interface circuit for negative input voltages up to a −50 V maximum. At V_I = 0 V a current flows from V_S through the 5.6 kΩ resistor and Z-diode BZX 97 C 5 V 6, which drives the transistor BC 108A into saturation. The input of the inverter FZH 201 is thereby grounded over the collector-emitter-region of the transistor BC 108A and an H-level appears at the output Q.

The diode BAY 44 conducts when the input voltage at I is negative. The center of the divider 2 x 5.6 kΩ now lies at a potential of about −0.7 V. The Z-diode is forward biased and the voltage at the anode of the BZX 97 settles to about 0 V. Thus the transistor BC 108A is blocked. An H-potential (V_S) is supplied to the input of the FZH 201 via the 10 kΩ resistor and the output Q changes to L. The maximum value of the H-input current to the FZH 201 is 1 μA, so that the voltage drop across the 10 kΩ resistor can be neglected. It is therefore possible to connect additional LSI-inputs at this resistor.

The R-C time constant (10 kΩ, 2.2 nF) increases the delay time of the interface stage thus providing a sufficient dynamic signal to noise ratio. However, for more stringent demands on the noise immunity the capacitance C can be increased.

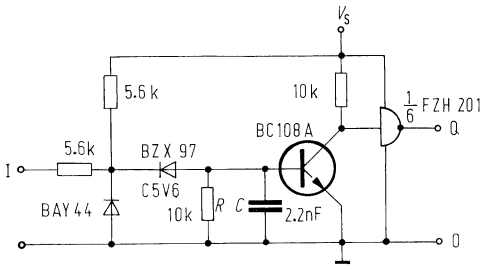


Fig. 5.4.4

5.4.5 Interface for Positive Input Voltages

Positive input voltages up to 150 V maximum can be applied at the input I of the interface stage shown in fig. 5.4.3. The diode BAY 45 with its high breakdown voltage protects the input of the inverter FZH 201 against overloading. When the BAY 45 diode is blocked, the resistor R = 10 kΩ supplies the required H-level (V_S) to the inverter input. The L-input voltage at I lies between 0 to 3,5 V. The diode BAY 45 between the gate input and ground is provided as a protection against negative voltages spikes.

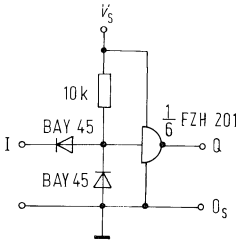


Fig. 5.4.5

5.4.6 Level Interface between LSL and TTL

The level converters FZH 161 and FZH 181 with open collector outputs were especially designed for these applications. The value of the collector resistor R_{TTL} and R_{LSL} is determined as follows:

$$\frac{5-0.4}{20-1.6\,N}\ \text{k}\Omega < R_{TTL} < \frac{5-2.4}{40\,n+80\,N}\ \text{M}\Omega$$

$$\frac{12(15)-1}{50-1.5\,(1.8)\,N}\ \text{k}\Omega < R_{LSL} < \frac{12(15)-10(12)}{250\,n+N}\ \text{M}\Omega$$

where n = number of AND-connections
N = number of attatched inputs

The selected resistance must have a value in between the upper and lower limits.

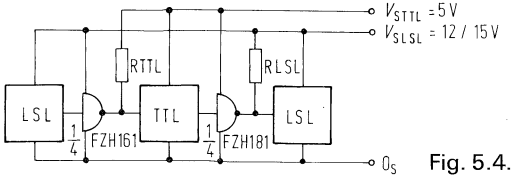


Fig. 5.4.6.

5.4.7 **Level Interface between LSL and MOS including CMOS**

Because of their compatible supply voltage levels, LSL and high voltage MOS circuits can easily be coupled if the usually negative MOS supply voltage is displaced as shown in fig. 5.4.7. LSL output and MOS input interface directly. The level interface LI between the MOS output and the LSL input depends on the MOS output structure. Push-pull-stages with an output resistance $R_Q < 3\ k\Omega$ (relative to V_{DD}) can drive one LSL input directly. Open drain stages with an output resistance $R_{QH} < 3\ k\Omega$ require a resistor connected to V_{GG} according to fig 5.4.7a. For high impedance MOS output a level interface as shown in fig. 5.4.7b must be provided. In both cases only one LSL input can be driven.

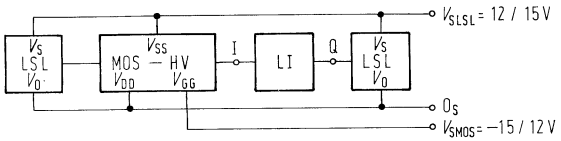


Fig. 5.4.7

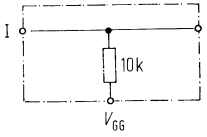


Fig. 5.4.7a

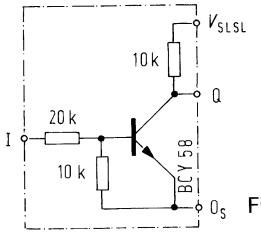


Fig. 5.4.7b

In cases where a supply voltage displacement is impossible, an interface as shown in fig. 5.4.7c can be used for high voltage MOS circuits. A transistor stage must be used at the input as well as the output to shift the level correspondingly.

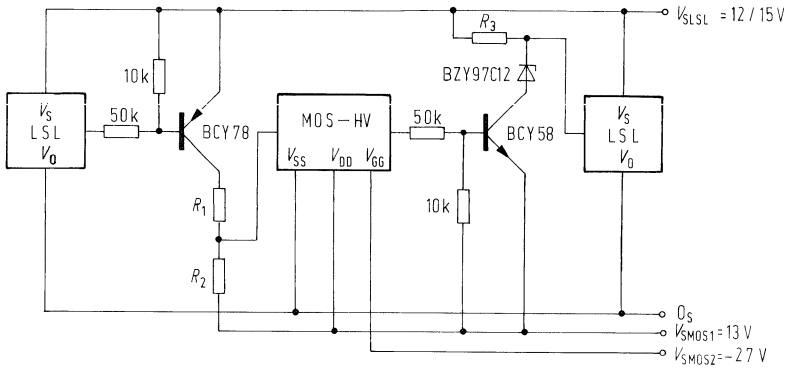


Fig. 5.4.7c

Low voltage MOS circuits are mostly TTL compatible. This means that the level converters FZH 161 and FZH 181 can be used as shown in fig. 5.4.7c. The dashed resistance R is required only for open drain outputs. The resistance R_{LSL} is dimensioned in accordance with the formula given in section 5.4.6.

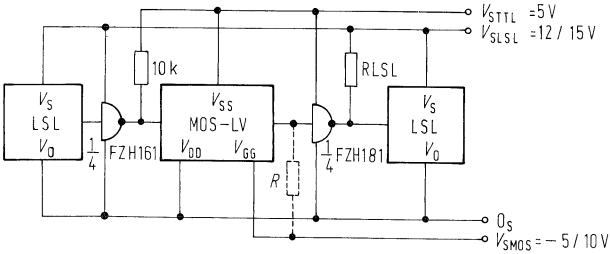


Fig. 5.4.7d

LSL and CMOS interface directly if the same supply voltage range is used as shown in fig. 5.4.7e. Any number of CMOS inputs may be driven by an LSL output. The current capability of the CMOS output determines how many LSL inputs may be connected. In general CMOS outputs supply enough current for one LSL input load, however the pertinent data sheet should always be consulted as CMOS output current capabilities vary to a large extent. For safe operation a CMOS buffer stage is recommended as an interface for LSL.

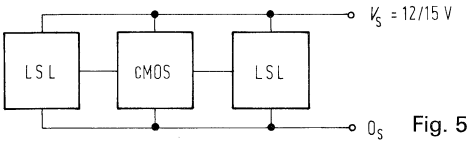


Fig. 5.4.7e

5.4.8 **Interface for Triacs**

Industrial control circuits often require the operation of triacs to control lamps and contactors. Fig. 5.4.8 shows the interface for the triac TXC 01. The circuit is suitable for control of load currents up to 6 A with an LSL gate. When the output of the FZH 201 is at an H-level, the transistor BC 108 conducts. The triac gate is thus supplied with a positive voltage and the triac starts conducting when the next positive halve wave arrives at the terminal V ~. As soon as the output of the FZH 201 switches to an L-level, the triac is turned off by the subsequent negative halve wave.
The triacs TXC 01 C 10 and TXC 01 E 10 are suitable for alternating voltages up to 100 V maximum. It is possible however to substitute the types TXC 01 C 20 to C 60 and TXC 01 E 20 to E 60. The maximum admissable alternating voltages then range from 200 to 600 V.

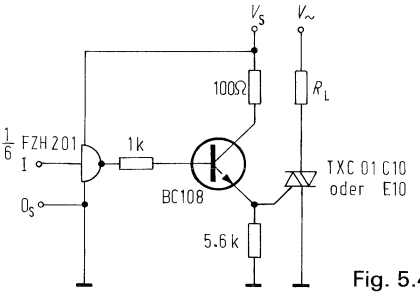


Fig. 5.4.8

5.4.9 **Output Power Stage**

Fig. 5.4.9 shows an output stage for load currents up to 6 A using a power darlington. The output transistor conducts when the input I of the inverter is supplied with an L-level. The output current of the FZH 201 is adjusted by a 1.5 kΩ series resistor to approximately 5to 6 mA so that the output voltage falls hardly below the H-limit. The serial diode BA 127 protects the output of the inverter FZH 201 from possible voltage transients. The 4.7 kΩ resistor ensures a defined switching threshold of the darlington stage.
The transistor BD 643 has a breakdown voltage of 45 V. For voltages of 60 or 80 V the final stage can be substituted by the types BD 645 and BD 647.

Recommended operating conditions:

Supply voltage:	V_S	12 V	15 V
Maximum output current:	I_L	5 A	6 A

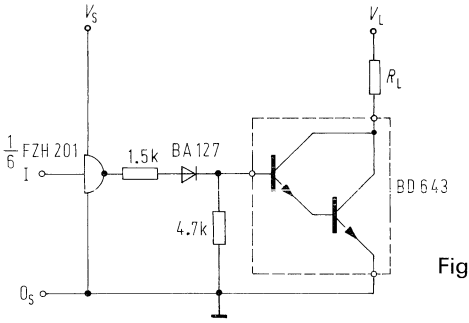


Fig. 5.4.9

5.4.10 **Output Power Stage with Short-Circuit-Protection**

Fig. 5.4.10 shows an output stage for commercial solenoid valves (V = 24 V, I= 0.5 A, R ~56Ω , L ~50 mH) using a power darlington. The solenoid is operated when an L-level is supplied to the input I of the inverter FZH 201.
If a short-circuit occurs between the supply voltage terminal V_L and the collector of the BD 675 the transistor BC 237 protects the power darlington against overloading. A voltage drop is generated at the emitter resistor R_E by the short-circuit current I_{SC}, which turns the transistor BC 237 on as soon as the base-emitter-voltage is attained.

The short-circuit-current is determined as follows:

$$I_{SC} \sim \frac{V_{BE}}{R_E} \; [A]$$

The transistor BC 237 turns on at a base-emitter-voltage V_{BE} ~ 0.55 V. Therefore the resistance R_E must be chosen in such a way that the short-circuit-current generates this voltage drop. Care must be taken to ensure that the voltage drop caused by the rated current I does not approach this value. An approximate value is given by the relation:
$I_{SC} = 1.1 \text{X } I$

Thus the resistor R_E is calculated as follows:

$$R_E \sim \frac{V_{BE}}{1.1 \text{ x } I} = \frac{0.55}{1.1 \text{ x } 0.5} = 1\Omega$$

The size of the heat sink and the short-circuit power dissipation determine the short-circuit duration. The power dissipation is approximately evaluated as follows:

$$P_{SC} \sim I_{SC} \text{ x } V_L \sim \frac{V_{BE}}{R_E} \; V_L = \frac{0.55}{1} \; 24 = 13 \; W$$

The thermal resistance of the heat sind required for continuous short-circuit is approximately:

$$R_{th} = 10 \; \frac{K}{W} \; .$$

The circuit in Fig. 5.4.10 is applicable for rated currents up to approx. 2 A. In this case the short-circuit power dissipation rises to a value of P_{SC} = 53 W and a heat sink with a thermal resistance of 2 K/W would be required for a continuous short-circuit.
Provided that the short-circuit is not repetitive and does not last more than 10 s, it has been found in practice that the thermal resistance can be 2 to 3 times higher than that calculated above. A trial run is however suggested in these cases.
The 2.2 kΩ resistor limits the output current of the inverter FZH 201 to a safe value. The serial diode BA 127 protects the output of the inverter from possible voltage transients.

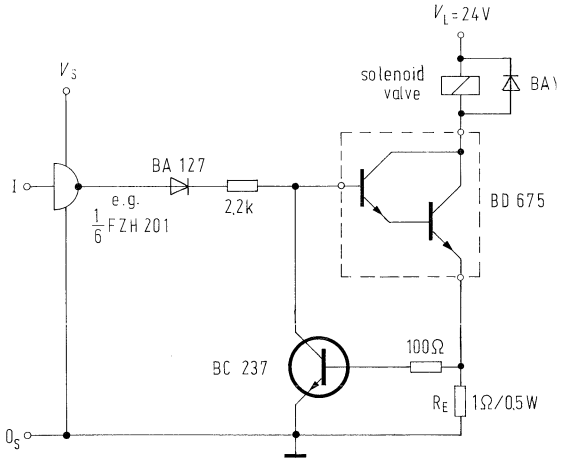


Fig. 5.4.10

5.4.11 **Output Stage for 100 to 300 V**

The output stage shown in fig. 5.4.11 is suitable for output voltages of V_L =100 to 300 V at load currents up to I_L = 0.5 A. The load is turned on by the power transistor BUY 35, when an H-level is applied to the input I of the inverter FZH 201. The dashed quenchdiode should be used for protection with inductive loads.
The load current is determined by the value of the resistor R which should be matched to the required load in order to keep its power dissipation low. The values of R = 8.2 kΩ and P = 2 W as specified in fig. 5.4.11 permit a load current of I_L = 0.3 A. The safe limit is $I_{Lmax.}$ = 0.5 A. A resistor with R = 3.3 kΩ and P = 5 W has to be used in this case. The voltage drop across the transistor BUY 35 when conducting is approximately V = 3 to 4 V. The power dissipation limits the output current to values below I_L = 0.3 A in cases where no heat sink is used. A heat sink with a thermal resistance of R_{th} = 30 K/W is required for load curents up to I_L = 0.5 A.

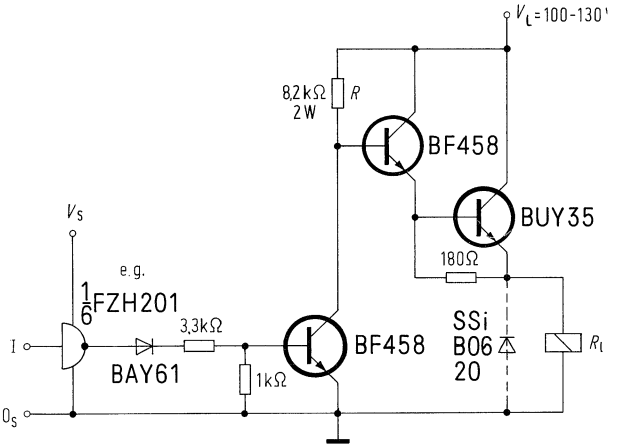


Fig. 5.4.11

5.5.1 Synchronous Counter with a 3:1 Division Ratio

Fig. 5.5.1 shows a synchronous divide-by-3-counter with the flipflop FZJ 121. The state of the counter is controlled by the Q and $\overline{Q}$ outputs and the J inputs. The connection between Q of FF1 and J of FF2 inhibits FF2 during every other clock pulse. The connection between $\overline{Q}$ of FF2 and J of FF1 blocks FF1 after the third pulse. The function table results as follows:

clock pulse	output Q_1	state* Q_2	corresp. decimal
1	L	L	0
2	H	L	1
3	L	H	2
4	L	L	0
⋮	⋮	⋮	⋮

* output state before the clock pulse

The clock frequency of the synchronous counter is equal to the clock frequency of the flipflops as the clock inputs are connected in parallel.

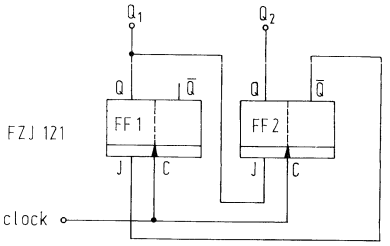


Fig. 5.5.1

5.5.2 **Synchronous Counter with a 4:1 Division Ratio**

A synchronous divide-by-4-counter with the flipflop FZJ 121 is shown in fig. 5.5.2. The connection between Q of FF1 and J and K of FF2 inhibits FF2 during every otherpulse. The following function table results:

clock pulse	output Q_1	state* Q_2	corresp. decimal
1	L	L	0
2	H	L	1
3	L	H	2
4	H	H	3
5	L	L	0
⋮	⋮	⋮	⋮

* output state before the clock pulse

The clock frequency of the connter is equal to the clock frequency of the flipflops.

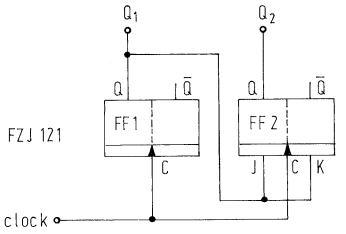


Fig. 5.5.2

5.5.3 **Programmable Counter and Divider**

Fig. 5.5.3 shows a counter the division ratio of which can be set to any decimal number between 1 and 15. The desired ratio is selected by means of the X-connections to the NAND-gate FZH 121. If, for example, X_3 and Q_3 as well as X_4 and Q_4 are tied and X_1 and X_2 are open, a reset signal is generated at $\bar{R}$ as soon as Q_3Q_4 = HH, i. e. after the 12th pulse at the clock input C of the counter FZJ 141.

Due to signal delay in the reset loop, output spikes may occur during reset mode. The counter output remains in its original state as long as the reset pulse propagates through the gate and the counter. This means that the counter returns to Q = L only shortly after the desired division ratio has been reached. These spikes may generate false information in stages operated by the counter outputs.

The following table gives the required X-connections with respect to the division ratio:

X_1	X_2	X_3	X_4	division ratio
O	O	O	O	–
C	O	O	O	1
O	C	O	O	2
O	C	O	O	3
O	O	C	O	4
C	O	C	O	5
O	C	C	O	6
C	C	C	O	7
O	O	O	C	8
C	O	O	C	9
O	C	O	C	10
C	C	O	C	11
O	O	C	C	12
C	O	C	C	13
O	C	C	C	14
C	C	C	C	15

C = connected
O = open

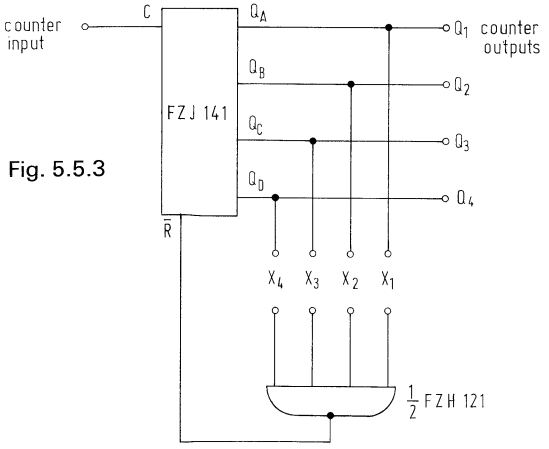


Fig. 5.5.3

5.5.4 **Reversible Decimal Counter with Preset**

Fig. 5.5.4 shows a synchronous reversible counter which has been devised for a minimum number of components. The additional JK inputs that are required for the FZJ 121 flipflops are obtained by a combination of diodes BAW 76.
The operating mode is selected by the input mode control MC. At MC = H the counter counts up. The NAND-gates connected with Q_1, Q_2, and Q_3 are enabled and control the JK inputs of the following flipflops FZJ 121. The NAND-gates operated by the inverter FZH 201 are simultaneously inhibited. The counter counts down at MC = L; the JK conditions now being derived from the $\bar{Q}$ outputs.

The truth table is as follows:

up

pulses at count input	mode control MC	carry C	outputs Q_4	Q_3	Q_2	Q_1			corresp. decimal	
1	H	L	L	L	L	L	H	L	11	0
2	H	L	L	L	L	H	L	L	10	1
3	H	L	L	L	H	L	L		9	2
4	H	L	L	L	H	H	L	L	8	3
5	H	L	L	H	L	L	L	L	7	4
6	H	L	L	H	L	H	L	L	6	5
7	H	L	L	H	H	L	L	L	5	6
8	H	L	L	H	H	H	L	L	4	7
9	H	L	H	L	L	L	L	L	3	8
10	H	H	H	L	L	H	H	L	2	9
11	H	L	L	L	L	L	H	L	1	0

Q_4	Q_3	Q_2	Q_1 outputs	C carry	MC mode control	pulses at count input

down

The carry pulse is generated by the gate FZH 231. This pulse controls not only the counting input of the following decade but inhibits also with J = L the second and third stage being in state Q_2 Q_3 = LL. This is necessary during up-counting, since due to conditions Q_1 = JK = H a state change of the second stage in possible, when the counter changes from Q_4 Q_3 Q_2 Q_1 = HLLH to LLLL (decimal 9 to 0). During counting down the same happens for the second and third stage, when the outputs change from Q_4 Q_3 Q_2 Q_1 = HHHH to LHHL, which corresponds to a change from decimal 0 to 9.
Counter preset is possible by the gate FZH 201 via the RS-inputs of the flip-flop FZJ 121.

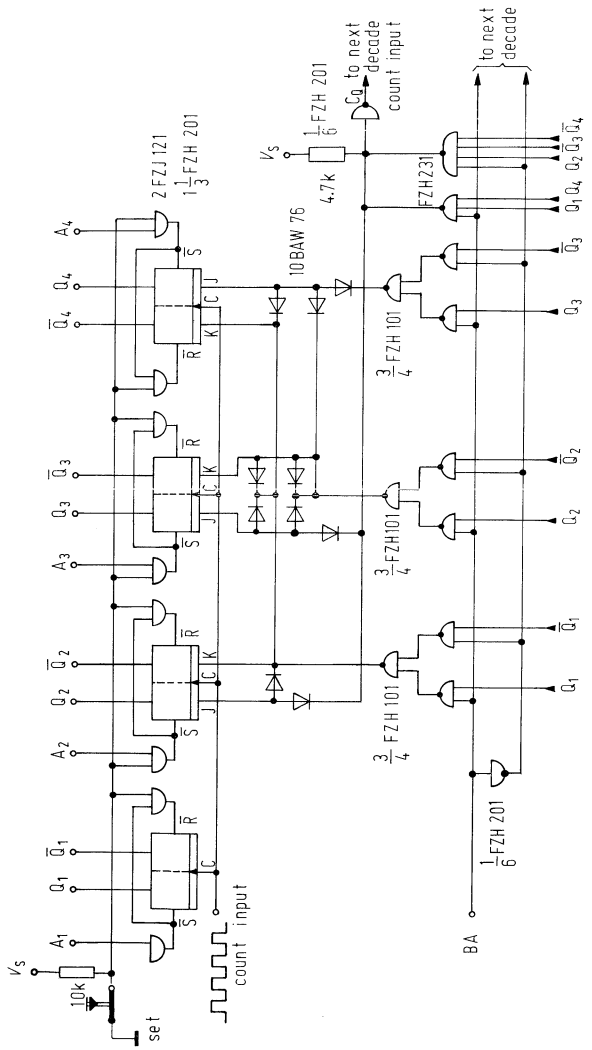

2 FZJ 121
1/3 FZH 201
1/6 FZH 201
Cq to next decade count input
to next decade
10BAW 76
4.7k
FZH231
3/4 FZH 101
3/4 FZH101
3/4 FZH 101
1/6 FZH 201
count input
set
10k
BA

Fig. 5.5.4

5.5.5 **Reversible Decimal Counter with High Noise Immunity**

The circuit shown in fig. 5.5.4 was devised with special regard to extreme noise conditions. Capacitors may be added to the flipflop FZJ 111 to increase the dynamic noise immunity to match existing conditions. Storage of false information and thereby false functions is safely avoided. For practical applications the additional capacitors may have a value of up to 3 nF. If greater values are used the operating speed of the counter becomes very slow. Theoretically the capacitance is not limited.
The truth table corresponds to the table given in 5.5.4.
Counter preset is possible by an additional gate FZH 201 via the RS inputs of the flipflops FZJ 111 as described in 5.5.4.

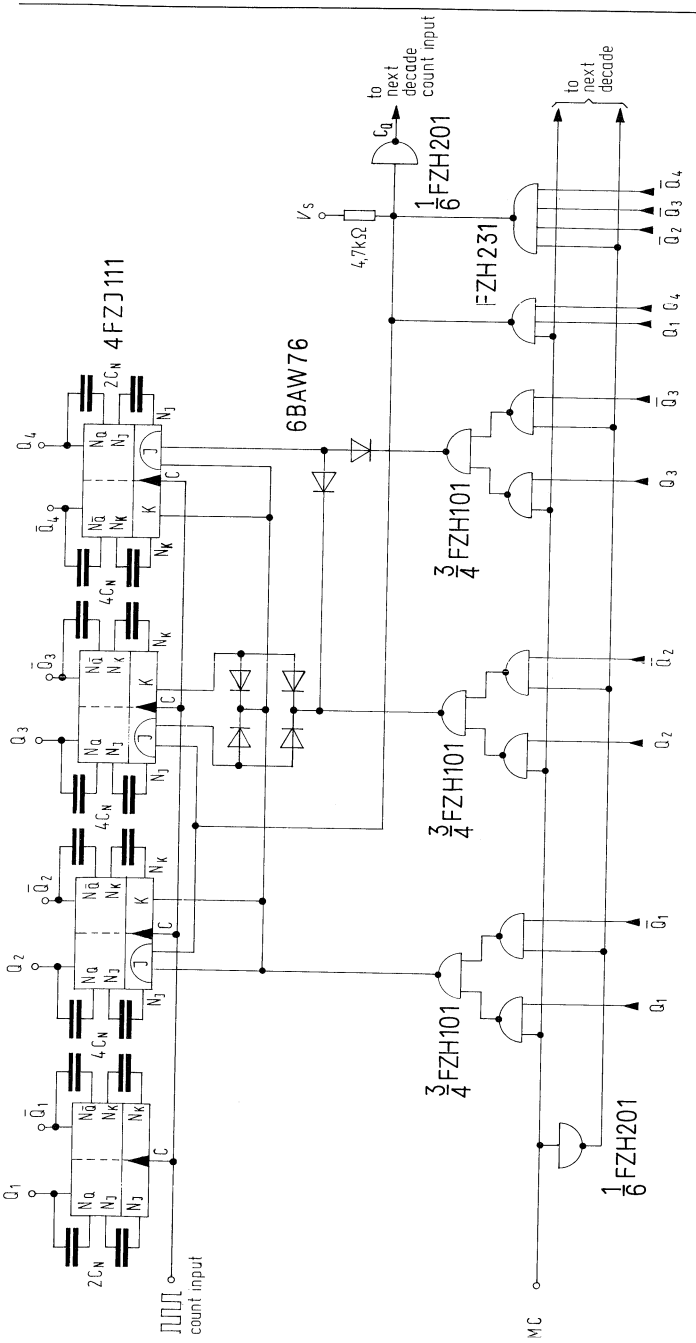

4FZJ111
6BAW76
4,7kΩ
V_S
to next decade count input
$\frac{1}{6}$FZH201
FZH231
$\frac{3}{4}$FZH101
$\frac{3}{4}$FZH101
$\frac{3}{4}$FZH101
$\frac{1}{6}$FZH201
to next decade
count input
MC

Fig. 5.5.5

5.5.6 **Reversible Binary Counter with Preset**

Fig. 5.5.6. shows a synchronous reversible counter with binary coded preset obtained at inputs A_1 to A_4. By opening the set button the respective gate inputs are enabled with an H-signal. The input condition A = L results in $\bar{R}$ = L at the reset input due to the dual inversion and in $\bar{S}$ = H at the set input on account of the single inversion. Thus the flipflop FZJ 121 is set to Q = L. Under the condition A = H the flipflops are preset to Q = H. The preset operation is independent of any other input condition of the counter since the $\bar{R}$ and $\bar{S}$ inputs of the FZJ 121 have priority.

The operating mode is selected by the mode control input MC. For counting up MC = H. Thus the NAND-gates connected to outputs Q_1, Q_2 and Q_3 are enabled and the NAND-gates driven by the inverter FLH 201 are inhibited. The JK information of the second flip-flop thus corresponds to the state at Q_1. At the third stage it is JK = Q_1 Q_2 etc. Down counting occurs at MC = L; the JK-conditions now being derived from the $\bar{Q}$ outputs.

The truth table of the counter is as follows

up

pulses at count input	mode control MC	outputs Q_4	Q_3	Q_2	Q_1			corresp. decimal
1	H	L	L	L	L	L	17	0
2	H	L	L	L	H	L	16	1
3	H	L	L	H	L	L	15	2
4	H	L	L	H	H	L	14	3
5	H	L	H	L	L	L	13	4
6	H	L	H	L	H	L	12	5
7	H	L	H	H	L	L	11	6
8	H	L	H	H	H	L	10	7
9	H	H	L	L	L	L	9	8
10	H	H	L	L	H	L	8	9
11	H	H	L	H	L	L	7	10
12	H	H	L	H	H	L	6	11
13	H	H	H	L	L	L	5	12
14	H	H	H	L	H	L	4	13
15	H	H	H	H	L	L	3	14
16	H	H	H	H	H	L	2	15
17	H	L	L	L	L	L	1	0
		Q_4	Q_3	Q_2	Q_1	MC mode control	pulses at count input	
		outputs						

down

An extension of the counter is easily possible by using the following rule for JK-conditions:
up counting:
$JK_n = Q_1\ Q_2\ Q_3\ Q_4 \ldots Q_{n-1}$
down counting:
$JK_n = \bar{Q}_1\ \bar{Q}_2\ \bar{Q}_3\ \bar{Q}_4 \ldots \bar{Q}_{n-1}$

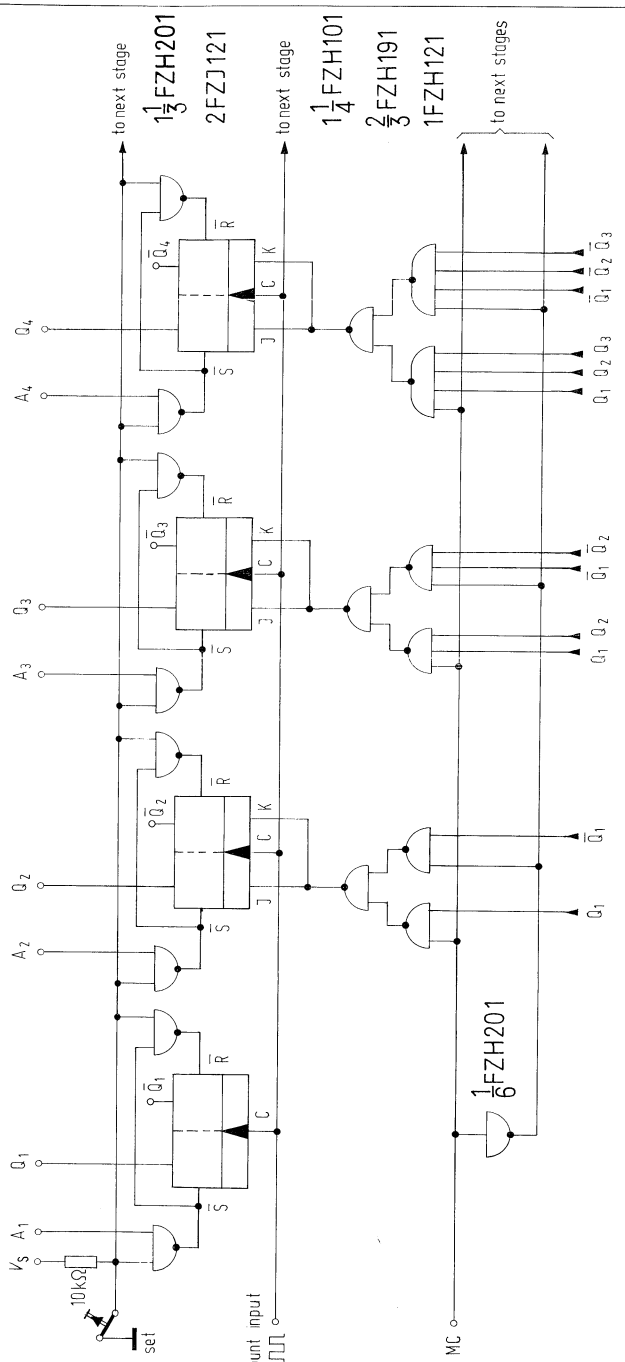

to next stage
1 1/3 FZH201
2FZJ121
to next stage
1 1/4 FZH101
2/3 FZH191
1FZH121
to next stages
V_S
A_1
Q_1
A_2
Q_2
A_3
Q_3
A_4
Q_4
10kΩ
set
count input
MC
1/6 FZH201
$\bar{Q}_1$
$\bar{Q}_2$
$\bar{Q}_3$
$\bar{Q}_4$
$\bar{R}$
$\bar{S}$
C
J
K
$\bar{Q}_1$
Q_1
$\bar{Q}_1 \bar{Q}_2$
$Q_1 Q_2$
$\bar{Q}_1 \bar{Q}_2 \bar{Q}_3$
$Q_1 Q_2 Q_3$

Fig. 5.5.6

5.5.7 **Synchronous Decimal and Binary Counter with 3 Stages**

Fig. 5.5.7 shows a counter chain with preset which operates as a decimal counter if the FZJ 141 is used and as a binary counter if the FZJ 151 is used. The preset inputs $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$ and the reset input $\overline{R}$ operate directly and have to be supplied with an H-signal during counting. This is achieved by connecting a hexinverter FZH 201 between the thumb-wheel-switches and the preset inputs. The strobe inputs of the FZH 201 are connected and controlled by an RS-flipflop with the circuit FZH 101. The RS-flipflop suppresses contact bounce of the set pushbutton. During steady state the inverters are inhibited by an L-signal at the strobe inputs. The strobe inputs change to an H-signal as soon as the set pushbutton is operated. The information selected by the thumb-wheel-switches is transferred to $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$. At the same time the pushbutton triggers the monostable multivibrator FZK 101 which resets the counters to Q = L. This is necessary since the preset inputs can be operated by L-signal only to switch the outputs Q to H-level.

The counter outputs are reset to Q = L by $\overline{R}$ = L. A correct storage of the information is assured only if set and reset inputs are simultaneously supplied with an L-signal for t = 1 µs and afterwards the reset input is returned to an H-signal at least 1 µs before the set inputs. These conditions are established by means of the monostable multivibrator. The adjusted delay time is $t_M = 0.7 \times R \times C = 0.7 \times 15 \times 10^3 \times 0.1 \times 10^{-9} = 1\ \mu s$. After this time has elapsed, the reset input returns to an H-signal whereas the BCD-information is present at A, B, C, D as long as the set pushbutton remains depressed.

The succeeding stages are controlled by the connection of the carry output C_Q to the enable input E and the carry enable input E_C.

The counter chain can be extended as desired in accordance with the pattern shown. However, the load factors of the RS-flipflop with the NAND-gate FZH 101 and the inverter connected to the output Q of the FZK 101 have to be observed. Any input of the counters FZJ 141 or FZJ 151 has to be supplied with a defined signal level; otherwise the correct function of the counter is not guaranteed. In fig. 5.5.7 this applies for the carry enable input E_C of the first stage.

The clock inputs of the counter stages are operated in parallel or synchronously. The typical operating frequency of the counters is 1.5 MHz.

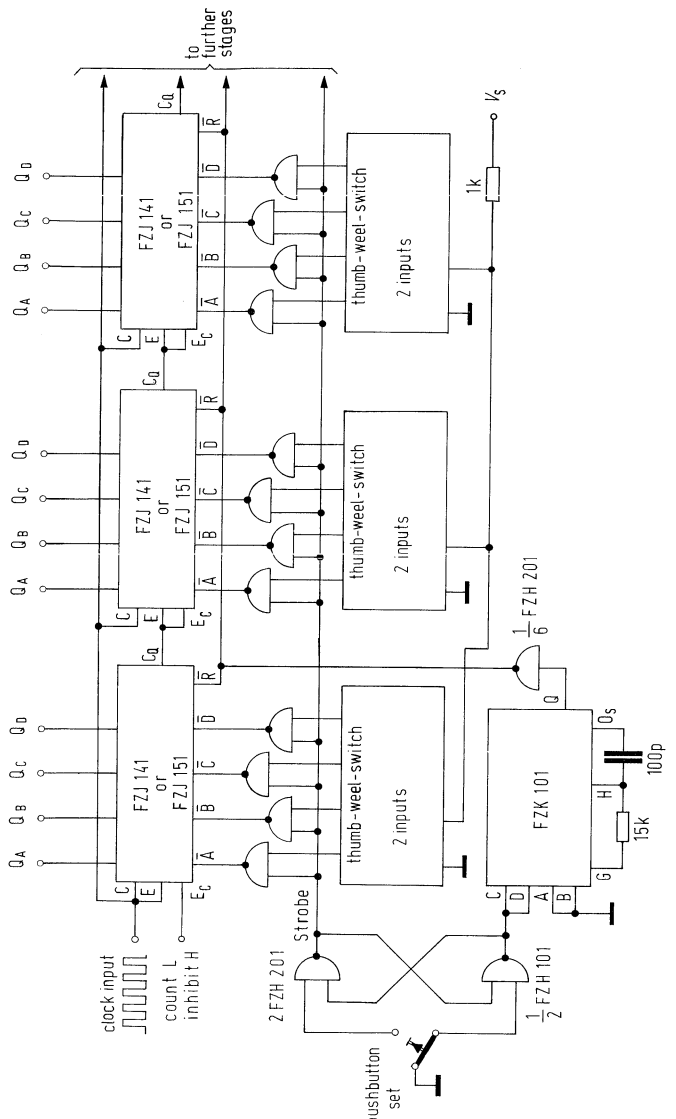

to further stages
FZJ 141 or FZJ 151
thumb-weel-switch
2 inputs
1k
V_S
$\frac{1}{6}$ FZH 201
FZK 101
100p
15k
clock input
count L
inhibit H
Strobe
2 FZH 201
$\frac{1}{2}$ FZH 101
pushbutton set

Fig. 5.5.7

5.5.8 **Decimal Counter with Direct Display**

Fig. 5.5.8a shows a decimal counter with scratch-pad memory, decoder, and display. The contents of the counter FZJ 141 are transferred to the scratch-pad memory FZJ 131 as soon as the strobe input is supplied with an H-signal. The decoder FZL 101, transforms the BCD-information into the decimal numbers and drives an indicator tube ZM 1180 or equivalent. The scratch-pad memory suppresses flicker of the indicator tube if strobed with a low frequency. Thus the display can be read easily.

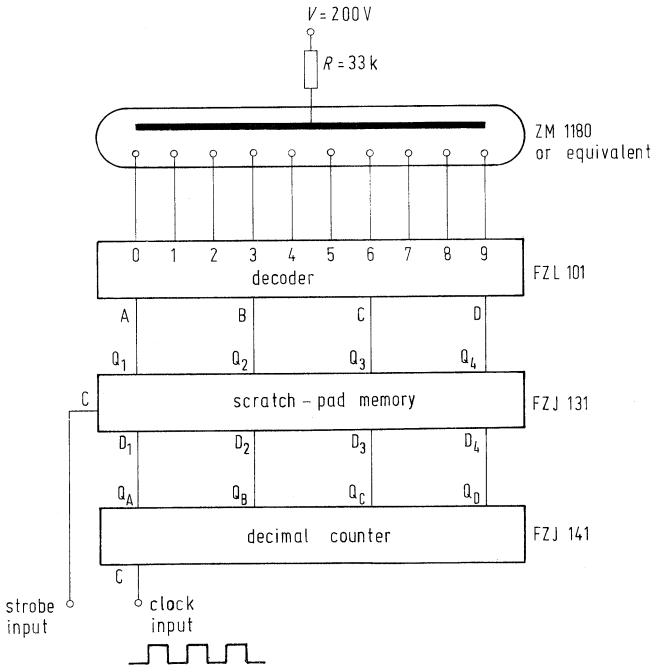


Fig. 5.5.8a
connect unused inputs to V_S

Fig. 5.5.8b shows the same circuit as before except that a 7-segment display is used. Tubes as well as light emitting diode arrays such as the CQY 22 may be driven by the decoder FZL 111. The series resistance has to be calculated in such a way that the maximum continuous output current I_Q = 20 mA per output of the FZL 111 is not exceeded.

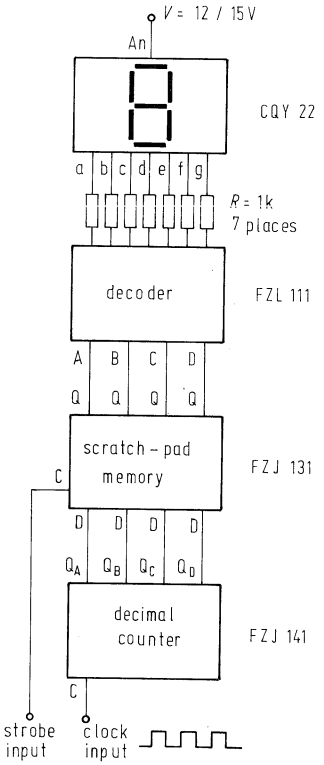


Fig. 5.5.8b
connect unused input to V_S

5.5.9 **Bidirectional Binary Counter for Control of Synchronization**

The counter shown in fig. 5.5.9 can be used for automatic synchronization of two parallel processes. For example, two projectors can be kept running synchronously. Thereby both projectors must produce a sequence of pulses with the same pulse width, the frequency being in proportion to the running speed. Regulation can be done on the basis of a reference pulse train. If a separate reference pulse train is not available, one of the two pulse sequences may be used as such. The deviation of the two pulse-trains can come up to 7 pulses. A deviation in running-speed produces the following error-signals:

$f < f_{norm}$, A_1 = L, A_2 = H
$f > f_{norm}$, A_1 = H, A_2 = L

In the case of equal frequencies
$f = f_{norm}$, A_1 = L, A_2 = L

If one pulse train should disappear, the second train must be stopped. The pulses still produced up to standstill (max. 7) are stored. Upon reappearance, this control is maintained until the preset number of the up down counter has been reached. An equivalent method is used in the reverse case. The total circuit comprises the up down counter, an input logic which prevents overlapping of the two pulse trains for comparison, furthermore a circuit performing preset of the updown counter to the number 8 = LLLH when the supply voltage is turned on, and the evaluation logic. The total circuit can be realized with 8 packages.

When the supply voltage is turned on, the up down counter is set to the decimal number 8. At first the output of the preset circuit is at logical L. The supply voltage applied to the integrating network R_1 C_1 changes this output level to H, after the threshold voltage of the first gate has been exceeded, and maintains this level. Only when the circuit is turned off and on again, this function will be repeated. The reference pulse train, or a pulse train which will be used as a reference, is present at input I_1; the pulse-sequence to be compared is at input I_2. If, for example, 3 pulses arrive at input I_1 during a certain time interval, whereas only 2 pulses appear at I_2, the counter will step to decimal 9. This decimal 9 acts upon the evaluation logic in such a way that output A_1 assumes an L-level and output A_2 an H-level. Consequently a two point control can be performed, correcting the source of the two pulses. In the reverse case the correction would be opposite.

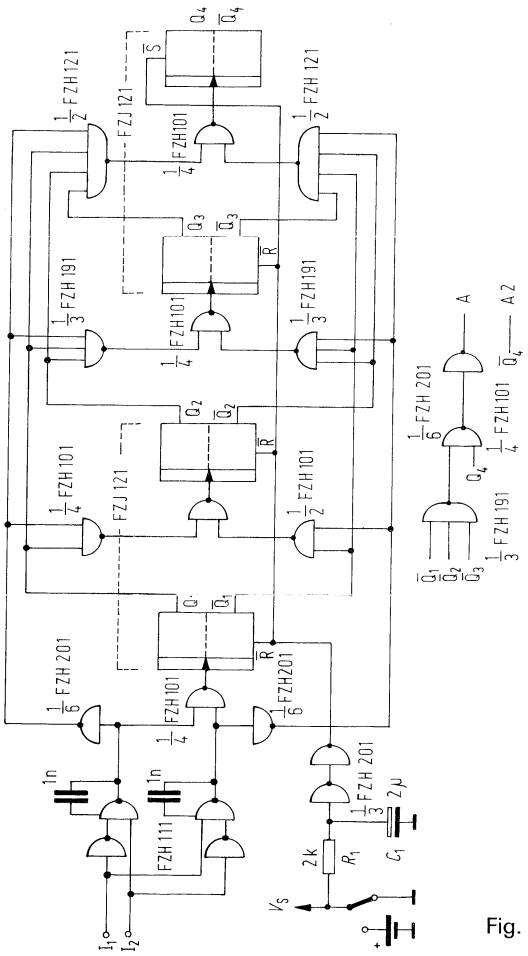

1/2 FZH121
FZJ121
1/4 FZH101
1/2 FZH121
1/3 FZH191
1/3 FZH191
1/4 FZH101
1/4 FZH101
FZJ121
1/2 FZH101
1/6 FZH201
1/4 FZH101
1/6 FZH201
1/3 FZH201
FZH111
1n
1n
2k
2µ
1/6 FZH201
1/4 FZH101
1/4 FZH101
1/3 FZH191
A
A2

Fig. 5.5.9

5.5.10 Ring Counter with RC-Coupled NAND-Gates

The control of manufacturing processes is often accomplished with ring counters or shift registers. Ring counters can be used as sequential controllers for work cycles which must be continually repeated. Shift register control is used for work programs that stop after completion. A circuit that accomplishes both functions is shown in fig. 5.5.10. The dotted connections indicate the circuit configuration for use as a ring counter (circulation register) and if these are not used the circuit operates as a shift register.

In the quiescent state the clock input must be at an L-potential. The outputs Q_1 to Q_4 are switched to H by momentarily closing the key R. Upon the closure of the key R all of the inputs of the gates I and I' receive an H-signal and an L-level (maximum 1.7 V) appears at the R-C components R = 3.3 kΩ, C = 100 nF.

The particular program is selected with the keys A to C. For example, when key A is closed the output of the FZH 121/I changes from L to H, the 100 nF capacitor is charged and Q_1 switches to L. The feedback from Q_1 to NAND-gate I ensures that this condition is maintained, when key A returns to its rest position.

The center point of the R-C time constant is connected to the input gate FZH 101/II. As soon as the capacitor is charged to an H-potential, the second stage can be triggered by an incoming clock pulse. The potential on the second R-C time constant changes from L to H and the output Q_2 switches to L. This signal change resets the first stage to Q_1 = H via the connection Q_2 and the Gate FZH 121/III. This process is repeated at every clock pulse. When the ring is closed (dotted connection) the information Q = L is conveyed to the first stage at every 4th, 8th and 12th pulse at C. This signal rotation can at any time be interrupted by key R. If the dotted connections are not made the information flow stops as soon as the condition Q_4 = L is obtained.

The R-C time constant determines the required clock pause t_p approximatly as follows:

$t_p = 0.7\ RC = 0.7 \times 3.3 \times 10^3 \times 100 \times 10^{-9} = 230 \times 10^{-6} = 230\ \mu s.$

The minimum clock period τ should be about $\frac{1}{10} t_p$ that is $\tau \sim 23\ \mu s$.

The operation of the register with an arbitrary clock pause is possible provided τ remains unchanged. Other values for τ require a corresponding adaption of the capacitance C.

A ring counter as shown in fig. 5.5.9 is also suitable for applications without clock pulse control. As long as the input C remains open stored information flows automatically. At the same time the input keys A to B initiate the signal circulation. The operating frequency can be varied with the capacitance C. The delay times of the NAND-gates FZH 101 and FZH 191 determine the minimum possible switching frequency. This limit is obtained with a capacitance of approximately C = 1 nF. The following calculation refers to the duration of the L-signal at the Q output of the particular stage under consideration.

$t_Q = 0.7\ RC = 0.7 \times 3.3 \times 10^3 \times 1 \times 10^{-3} = 2.3 \times 10^{-6} = 2.3\ \mu s.$

A realistic capacitance C determines the maximum switching frequency since the required L-input current to the clock gate limits the resistor value in the typical case to R = 3.3 kΩ and in the worst case to $R_{max} \leqq 1.8$ kΩ

A shift register which switches on automatically can also be achieved using the circuit in fig. 5.5.10. For this particular application the terminal C is not used and the clock gate FZH 101/IV and the dotted connection are also not required. The input belonging to the NAND-gate I remains open.

Any number of desired stages can be included in the shift register. It is possible to set Q = L for each second stage and shift the information simultaneously.

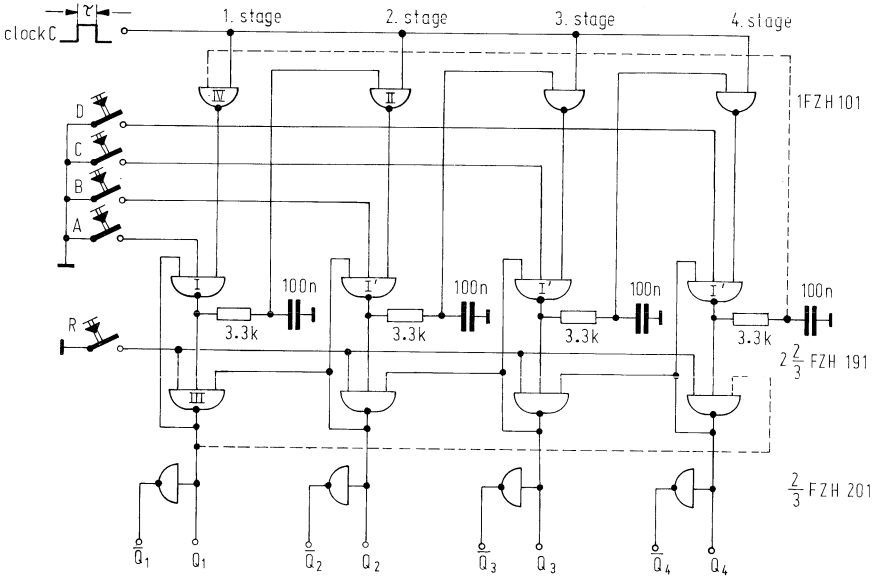

clock C
1. stage
2. stage
3. stage
4. stage
1FZH 101
D
C
B
A
R
100n
3.3k
2 2/3 FZH 191
2/3 FZH 201

Fig. 5.5.10

5.5.11 **Bidirectional Shiftregister**

The shiftregister shown next consists of 6 JK flipflops. Each clock pulse shifts the information loaded into the register by one bit to the right or to the left from its initial position. This kind of recirculation register is frequently used for the control of tooling machines.
When the supply voltage is turned on, the integrating network R_1/C_1 causes the first and the last flipflop to be set to an H-level and the remaining flipflop to an L-level.
The register shifts to the right if the input MC is supplied with an H-level. In this case one input each of the odd numbered gates is supplied with an H-signal. The output of the preceding flipflops are connected to the second input of these gates. When the output of the preceding flipflop is at an H-level, the output of gate 1, for example, will assume an L-level. By means of the succeeding NAND-gate and the inverter, the input conditions of the first flipflop will be J = H and K = L.
The flipflop will remain at Q_A = H at the following clock pulse due to this input condition. If the information at the second input of gate 1 changes to an L-level, an H-level will result at its output. Because there will also be on H-level at the output of the second gate, the input conditions of the first flipflop will now be J = L and K = H. The flipflop will change to Q_A = L at the next clock pulse due to this condition. The operation of the other flipflops can be determined in a similar way.
Left shift operation is achieved by an L-signal at MC. During left shift operation the information from the outputs is transferred to the inputs of the preceding flipflop by means of the even numbered gates. The odd numbered gates are blocked by an L-level.

Truth table for right shift operation:

	mode control	outputs of the flipflops					
	MC	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F
Initial state	H	H	L	L	L	L	H
1st clock	H	H	H	L	L	L	L
2nd clock	H	L	H	H	L	L	L
3rd clock	H	L	L	H	H	L	L
4th clock	H	L	L	L	H	H	L
5th clock	H	L	L	L	L	H	H

Truth table for left shift operation:

	mode control	outputs of the flipflops					
	MC	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F
Initial state	L	H	L	L	L	L	H
1st clock	L	L	L	L	L	H	H
2nd clock	L	L	L	L	H	H	L
3rd clock	L	L	L	H	H	L	L
4th clock	L	L	H	H	L	L	L
5th clock	L	H	H	L	L	L	L

Any desired program can be realised if the set and reset inputs $\bar{S}$ and $\bar{R}$ of the flipflops FZJ 121 are wired correspondingly.

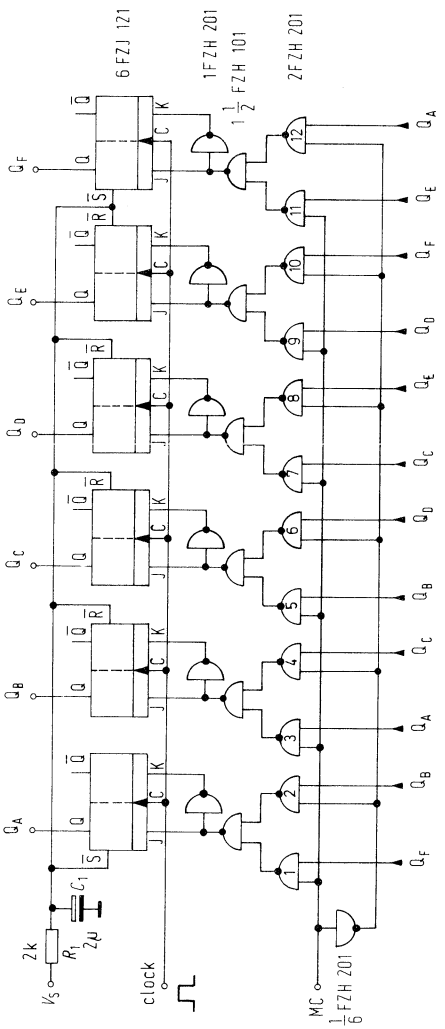

6 FZJ 121
1 FZH 201
1 1/2 FZH 101
2 FZH 201
Q_A
Q_B
Q_C
Q_D
Q_E
Q_F
2k
R_1
2µ
C_1
V_S
clock
MC
1/6 FZH 201

Fig. 5.5.11

5.5.12 **Input Register**

Fig. 5.5.12 shows an input register with the shift register FZJ 161 with 16 stages. As soon as the start key is activated, the monostable multivibrator FZK 101 is triggered. The resulting output pulse resets the shift registers FZJ 161, the control counter FZJ 151, and the control flipflop FZJ 101 to Q = L. The set inputs of the shiftregisters FZJ 161 are enabled after a short delay caused by the capacitively delayed NAND-gate FZH 111. This is necessary as a proper information storage is assured only if set and reset inputs are simultaneously supplied with an L signal for t = 1 μs and afterwards the reset input is returned to an H-signal at least 1 μs before the set input. Thus the information from the select switches S_1 to S_{16} at the preset inputs A, B, C, D is stored in the register flipflops. The Q outputs serve as a status indicator by means of light emitting diodes LD 468. When the start key is released, the input gate FZH 191 is activated and clock pulses are supplied to the clock inputs of the register and the counter. The binary counter FZJ 151 clocks the control flipflop FZJ 101 via the carry output C_Q. The control flipflop changes to Q = H after the 16th clock pulse and blocks the input gate FZH 191. The end of the sequence is indicated by another light emitting diode. The information stored in the register is retained as the register is retained as the register the serial output SQ and the serial input SI. The control circuit can be disabled by the repetition switch S. The register circulates the information as long as the switch is in the position ground (L-signal).

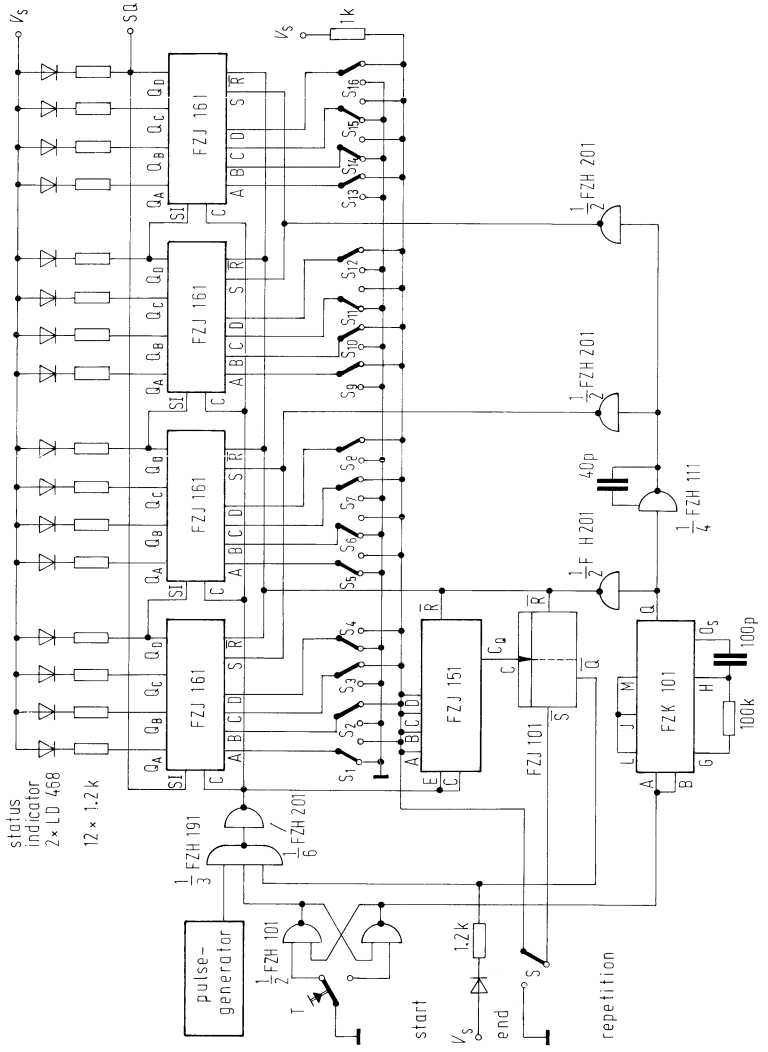

V_S
SQ
1k
FZJ 161
FZJ 151
FZJ 101
FZK 101
FZH 191
FZH 201
FZH 101
FZH 111
FH 201
40p
100p
100k
1.2k
status indicator 2× LD 468
12 × 1.2 k
pulse-generator
start
end
repetition

Fig. 5.5.12

5.6.1 **Halfadder**

Fig. 5.6.1 shows a halfadder which is simply realised by an exclusiv-OR-gate FZH 271. The truth table is as follows:

inputs A	inputs B	output Q
L	L	L
L	H	H
H	L	H
H	H	L

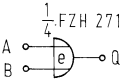


Fig. 5.6.1

5.6.2 **Halfadder with Carry Output**

If an AND-gate is added to the circuit of fig. 5.6.1, a carry signal is generated at the output C_Q. The truth table is now as follows:

inputs A	inputs B	sum output Σ	carry output C_Q
L	L	L	L
L	H	H	L
H	L	H	L
H	H	L	H

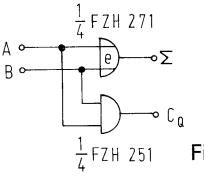


Fig. 5.6.2

5.6.3 **Fullader**

A fulladder can be realised by means of two halfadders according to fig. 5.6.3a. An additional gate is required for the generation of the final carry signal. The circuit is simplified if NAND-gates are used instead of AND-gates for this purpose.

inputs A	inputs B	inputs C_I	sum output Σ	carry output C_Q
L	L	L	L	L
L	H	L	H	L
H	L	L	H	L
H	H	L	L	H
L	L	H	H	L
L	H	H	L	H
H	L	H	L	H
H	H	H	H	H

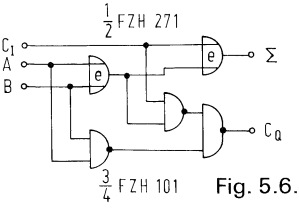


Fig. 5.6.3a

An adder network of n bits is formed by cascading the carry inputs and outputs as shown in fig. 5.6.3b

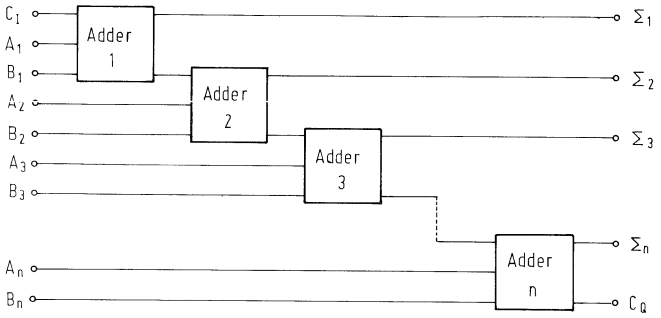


Fig. 5.6.3b

5.6.4 **Comparator for n Bits**

A comparator which supplies the information A = B and A ≠ B is shown in fig. 5.6.4. No indication is given whether A is greater or smaller than B. The actual comparison is performed by the exclusive-OR-gate FZH 271. After having been inverted, the information is combined by the NAND-gate FZH 171. Thus output Q indicates the relation between A and B as follows:

Q = L, A = B
Q = H, A < B or A > B

The circuit can be expanded to n bits by means of additional diodes, excluive-OR-gates, and inverters at the expander input N_1 of the FZH 171.

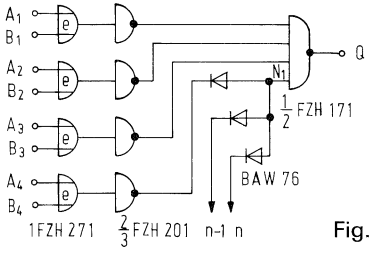


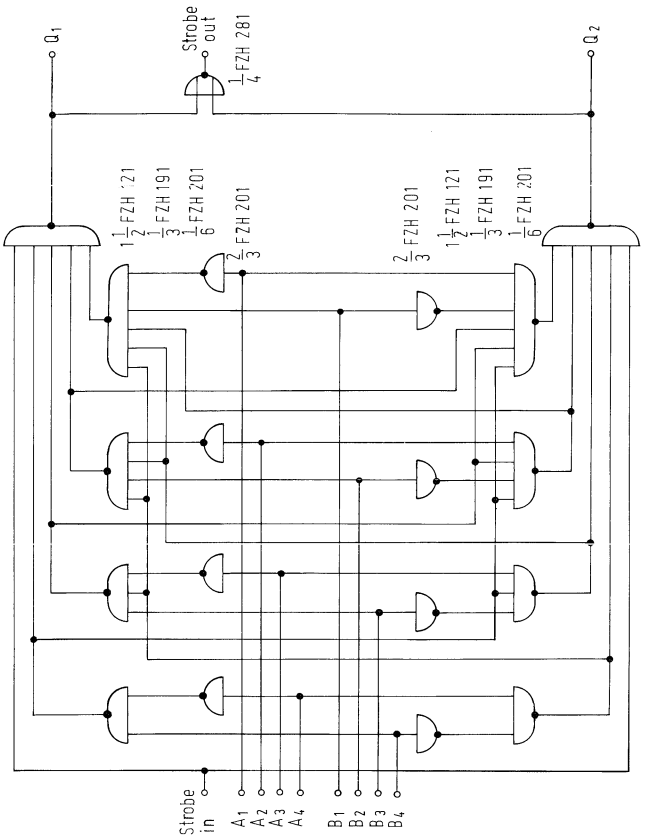
Fig. 5.6.4

5.6.5 **4-Bit-Comparator with Strobe**

A 4-bit-comparator which supplies the information A = B, A < B, and A > B is shown in fig. 5.6.5. Strobe inputs and outputs permit an expansion to n bits. The comparison is performed serially in such a way that the outputs of the gates for the comparison of A_4 and B_4 also control the inputs of the gates for the comparison of A_3 and B_3 and so on. In this way a minimum number of components is needed. However, the speed of the comparator is reduced by this method.
The outputs Q_1 and Q_2 indicate the comparison as follows:

inputs A	B	strobe in	outputs Q_1	Q_2	strobe out
A <	B	H	H	L	L
A >	B	H	L	H	L
A =	B	H	L	L	H
X	X	L	H	H	L

X = L or H-signal


Q1
Strobe out
1/4 FZH 281
Q2
1 1/2 FZH 121
1 1/3 FZH 191
1/6 FZH 201
2/3 FZH 201
2/3 FZH 201
1 1/2 FZH 121
1 1/3 FZH 191
1/6 FZH 201
Strobe in
A1
A2
A3
A4
B1
B2
B3
B4

5.7 Pulse Circuits

5.7.1 **Delay Circuits**

The delay capability of LSL-gates can be used to design simple delay circuits for delay times up to approximately 1 s. Two basic variations are possible. Fig. 5.7.1 shows a delay circuit with the AND-gate FZH 251. The length of the delay is determined by the capacitance added to first gate. The action on a positive pulse at the input I is shown in fig. 5.7.1a. It can be seen that leading edge of the output pulse is delayed while the trailing edge coincides with the input pulse. The case of a negative pulse is shown in fig. 5.7.1b. Here the leading edges of input and output pulse coincide while the trailing edge of the output pulse lags.

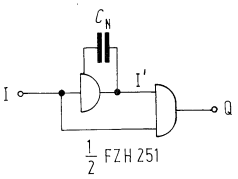


Fig. 5.7.1

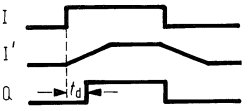


Fig. 5.7.1a

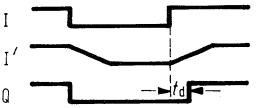


Fig. 5.7.1b

A delay circuit with the OR-gate FZH 291 is shown in fig. 5.7.1c. The action of this circuit is exactly opposite to the circuit shown above. The trailing edge of a positive pulse lags whereas the leading edge of a negative pulse is delayed. The corresponding pulse diagrams are given in fig. 5.7.1 d and e.

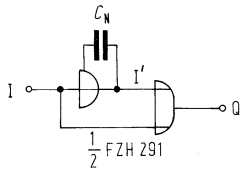


Fig. 5.7.1c

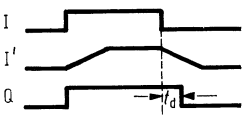


Fig. 5.7.1d

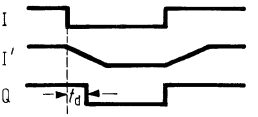
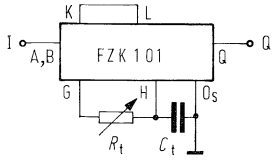


Fig. 5.7.1e

Circuits which produce a lag of the leading and the trailing edges can be realised by aserial connection of the circuits shown above.

5.7.2 **Delay Circuits**

Delay times with a wide variation and a great accuracy can be generated by the timing circuit FZK 101. The delay time is determined by the timing components R_t and C_t. The resistance R_t should be kept within the limit of 40 to 200 kΩ for great accuracy. The leakage current of large capacitors on the timing may also be of adverse influence. Fig. 5.7.2 shows a delay circuit for the leading edge of positive input pulse. A circuit for negative pulses is given in fig. 5.7.2a. The additional inverter FZH 201 establishes the correct phase relation between input and output.



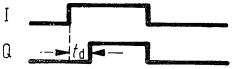
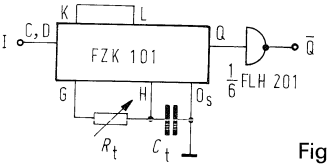


Fig. 5.7.2



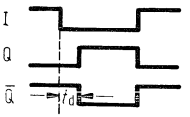
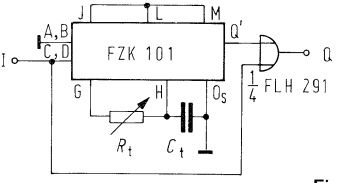


Fig. 5.7.2a

Additional logic is required for the delay of the trailing edge. Fig. 5.7.2b shows a circuit for positive pulses and fig. 5.7.2c for negative pulses.



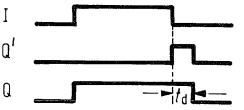
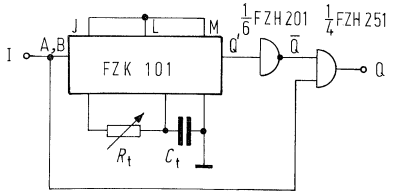


Fig. 5.7.2b



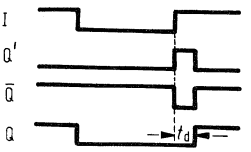
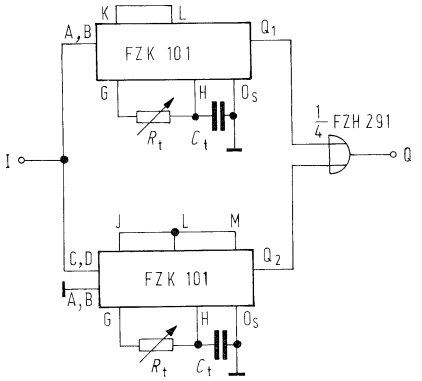


Fig. 5.7.2c

A circuit the delay of which can be independently adjusted for the leading and the trailing edge is formed by combining the above mentioned circuits as shown in fig. 5.7.2d.The upper FZK 101 is triggered by the L-H transition of the input signal and the lower FZK 101 by the H-L transition. Both outputs are connected by an OR-gate. The delay circuit is intended for positive input pulses. A corresponding combination can be made for negative pulses.



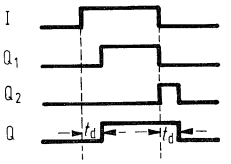
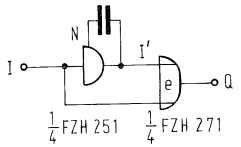
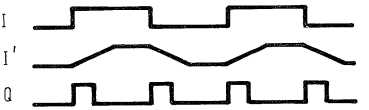


Fig. 5.7.2d

5.7.3 **Pulse Doubling Circuit**

If an exclusive-OR-gate is used in conjunction with a delayed gate, a circuit which generates one output pulse for every input transition results. In this way a simple circuit which doubles the input frequency can be realised.





5.7.4 **Monostable Multivibrator**

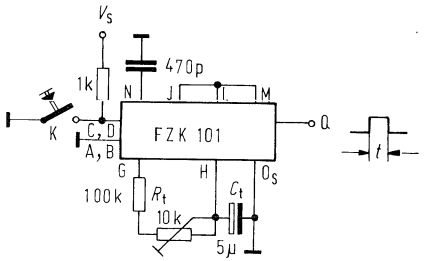
The timing circuit FZK 101 can be used as a monostable multivibrator, as a pulse delay and pulse reduction circuit. The desired function is selected by connections between the terminals J, K, L, M. Fig. 5.7.4 shows as an example the application as a monostable multivibrator with J, L, and M connected. The FZK 101 is triggered by closing the key K. K has to be free of chatter to ensure a proper release.

The time delay is determined by the time constant at the terminals G, H, and O_S. Normally a fixed resistor is used for coarse adjustment and a trimmer with a value of 10% of the fixed resistor for fine adjustment. The timing resistance may vary between 5 and 500 kΩ, however, for greater accuracy a value between 40 and 200 kΩ is recommended. The accuracy is generally better for a smaller timing resistance. The capacitance is arbitrary and permits the delay time to be adjusted over a wide range. The leakage current of the capacitor must be inversely proportional to the resistance R_t, i. e. below 0.5 μA at R_t = 500 kΩ and below 5 μA at R_t = 5 kΩ.

The delay time is determined by:

$t = 0.7 \times R \times C = 0.7 \times 105 \times 10^3 \times 5 \times 10^{-6} = 367.5$ ms

The trimmer enables an adjustment in the time t of about ± 5%. This corresponds to about the same deviation which can be expected in the production, when the timing components have a tolerance of ± 1%.
A 470 pF capacitor at the N-terminal increases the dynamic noise immunity.



5.7.5 Functional Extension of the Timing Circuit FZK 101

The upper value of the timing resistor of the FZK 101 is restricted to 500 kΩ. This means that large capacitors are needed if the time delay becomes rather great. This disadvantage can be avoided with an additional circuit as shown in fig. 5.7.5. It can be used with any operating mode.
The permissible resistance range is extended to a lower limit of R_t = 1 kΩ and to a higher one of R_t = 10 MΩ. In fig. 5.7.5a the resulting output pulse duration at monostable operation $t_Q = f(R_t)$ is shown. The parameter is C_t with values between 1 nF and 10 µF. The relation $t_Q = 0.7 \times R_t \times C_t$ s for calculating the output pulse duration is not effected by this additional circuit.
If the resistor R_t is replaced by a constant voltage source V_t with a low internal impedance, then the output pulse duration t_Q is variable with this voltage. The equivalent resistance $R_t' = 0.7 \times R_t$ as a function of a certain voltage V_T is shown in fig. 5.7.5b. If the voltage is for instance V_t = 3 to 4 V, R_t' = 0.7 x R_t = 1.6 to 3.2 kΩ follows. Assumed that C_t is 1 nF output pulse duration may be varied as follows:

$t_{Q1} = 0.7 \times R_t \times C_t = 1.6 \times 10^3 \times 10^{-9} = 1.6\,\mu s$

$t_{Q2} = 0.7 \times R_t \times C_t = 3.2 \times 10^3 \times 10^{-9} = 3.2\,\mu s$

and $t_{Q2} : t_{Q1} = 2 : 1$

The additional circuit operates as a constant current source in such a way that the current flowing through resistor R_t is the same as the one charging the capacitor C_t. It has to be considered that the resistor R_t which can be any resistive component, e.g. NTC-resistor, PTC-resistor, magneto resistor or optovoltaic cell, does not fall below a value of R_t = 1 kΩ. This means that a positive voltage V_t = 2.5 V is allowed as a minimum value for operation with a constant voltage source. Below these limits the output of FZK 101 assumes the state Q = H.

Operation of the FZK 101, however, is admissible to values of V_t = 0 V and R_t = 0 Ω. Only negative values of V_t destroy the FZK 101. The upper limit of the capacitance is determined by the amount of the capacitor leakage current. Electrolytic capacitors with a capacitance of 100 µF may have leakage currents in the order of the charging current of this circuit. Therefore the correct function is only guaranteeed at values of C_t < 100 µF.
Two 100 Ω series resistors reduce the influence of temperature variations.

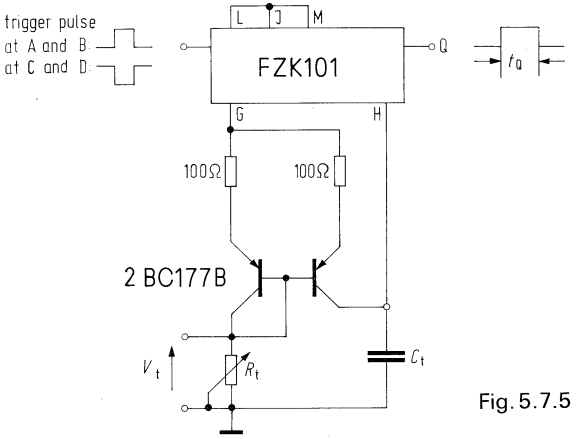


Fig. 5.7.5

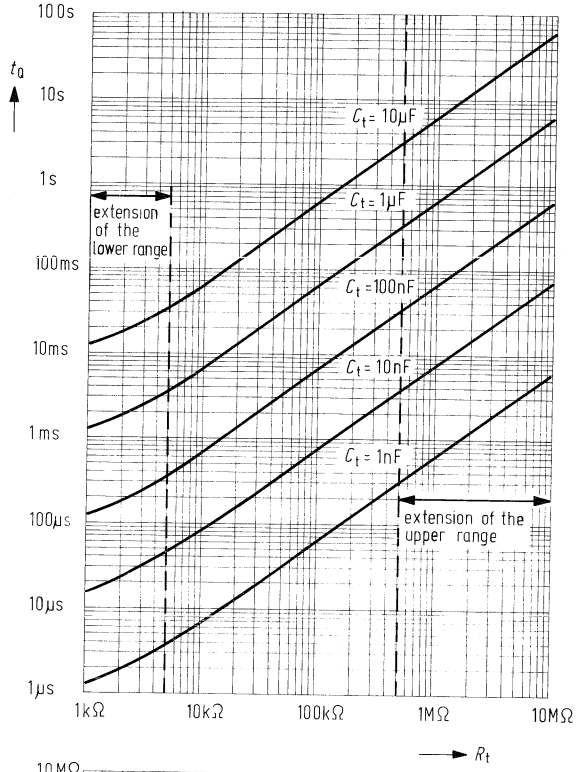


Fig. 5.7.5a

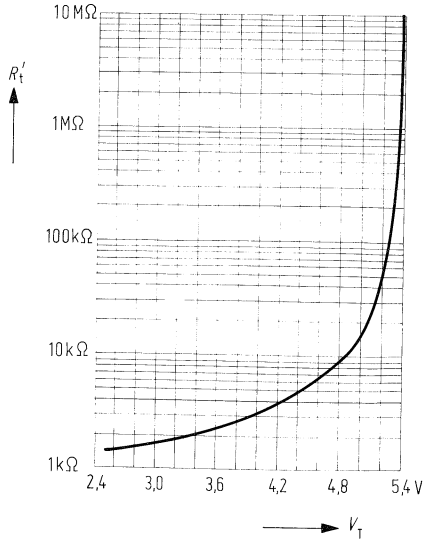


Fig. 5.7.5b

5.7.6 **Pulse Sequence Monitor with the Timing Circuit FZK 101**

Fig. 5.7.6 shows a simple pulse sequence monitor with the FZK 101 as a monostable multivibrator. As long as the pulses arriving at input I have an approximately uniform duty cycle, an H-signal will be present at output Q. The output changes to an L-signal if one of the pulses is missing. The first monostage is blocked via the connection from output Q to input C. Another monitoring process is initiated by the operation of the breakkey K.
The function of this circuit is as follows: The first leading edge of a pulse at I triggers the first FZK 101. Output Q_1 switches to an H-level and produces via the gate FZH 111/I an H-signal at the output Q. When the delay time of this monostable multivibrator has expired, Q_1 changes from an H to an L-level and releases the second FZK 101. The signal change at Q_2 causes Q to remain at an H-level by means of the gate FZH 111/II. The 15 pF integrating capacitor lengthens the propagation delay times of the NAND-gate I to such an extent that the turn-on delay of the second FZK 101 is effectively cancelled. An L-spike is thus safely avioded at output Q.
The R_tC_t time constant determines the delay time t of the monostable multivibrator such that:

$t = 0.7 \times R \times C$

Consideration of the pulse pause t_p and the pulse width t_w at the input I yields the following conditions for the delay time t:
$t_{min} = 1/2\ (t_p + t_w)$ and $t_{max} = t_p + t_w$

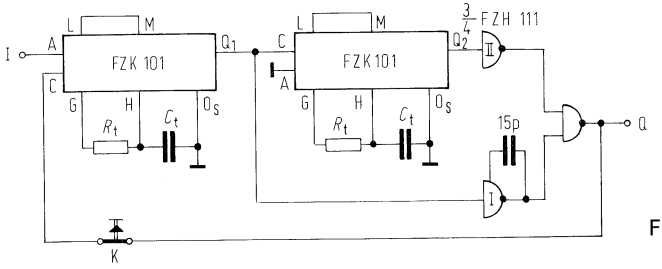


Fig. 5.7.6

5.7.7 **Pulse Generator**

Fig. 5.7.7 shows a self starting pulse generator with an LSL-NAND-gate FZH 101. The function of the generator is based on a steady polarity inversion of the capacitor voltage caused by the negator II. The change occurs when the capacitor voltage reaches the threshold voltage of the inputs of the gates I and II.
The oscillating frequency f of the generator depends on the RC time constant. A frequency variation with a ratio of approximately 1 : 3 is possible by means of the trimmer P. The frequency is determined by

$$f = \frac{1}{2\,RC}$$

The following variation results for the endpositions:

$$f_{min} = \frac{1}{8{,}3 \cdot 10^3 \cdot 0{,}1 \cdot 10^{-6}} = \sim 1{,}2\,\text{kHz and } f_{max} \sim 3\,\text{kHz}$$

The maximum possible frequency is about 0.5 MHz. It is given by the propagation delay of the gates. The input $\overline{I}$ is provided for interruptions of the generator. An L-level at $\overline{I}$ ensures a constant L-signal at the output Q.

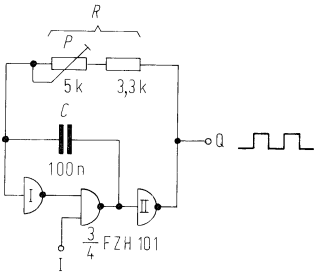


Fig. 5.7.7

5.7.8 **Pulse Generator**

An inexpensive selfstarting oscillator can be realised with the Schmitt-Trigger FZH 241 according to fig. 5.7.8. A feedback resistor R and a capacitor C to ground roughly determine the pulse duration as follows:

$t = k \times R \times C\,s$

The factor k depends on the resistance R and can be derived from the typical curve of fig. 5.7.8. The recommended resistance variation is 0.2 to 10 kΩ. Values below 0.2 kΩ exceed the output load factor of the FZH 241. Values above 10 kΩ reduce the charging and discharging currents to such an extent that frequency stability of the oscillator is no longer guaranteed. Any capacitor of an arbitrary value may be used.
The lowest possible pulse duration is approximately t = 1 µs due to the propagation delay of the FZH 241.
A supply voltage variation from 11 to 17 V will increase the pulse duration by approximately 10%. A temperature variation from 20 °C to −30 °C will reduce the pulse duration by approximately 5%. A temperature variation from 20 °C to 70 °C will increase the pulse duration by 10%.
A 1 µF capacitor should be connected directly to the supply voltage terminals to suppress possible overshooting.
The second Schmitt-Trigger is used as a pulse shaper. Generally it is required only for feedback resistors below R = 4 kΩ.

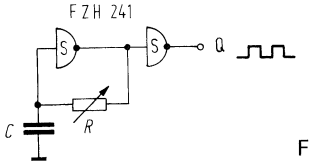


Fig. 5.7.8

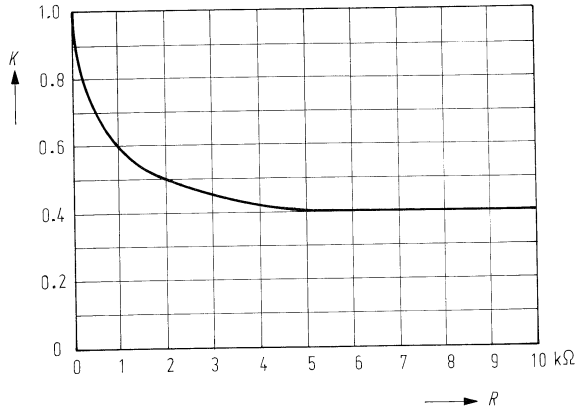


Fig. 5.7.8a

5.8 Control Circuits

The LSL-series FZ 100 is ideally suited for applications in control circuits. In the following several practical circuits are given as an example. Due to its high static and dynamic noise margin, the LSL-series has been used successfully in such circuits as elevator controls, process controls, in any kind of machine controls for grinding machines, tooling machines, stamps, and presses, to name just a few examples.

5.8.1 **Welder Timing Control**

Electronic time limiters with electronic power switches have found universal application in the field of resistance welding. The power switch at the transformer primary winding has a combined resistive-inductive load. If the welding transformer is not turned-on in a fixed and proper phase condition, a high switching peak current may initially occur and reduce to a normal level not before several cycles have passed. It is therefore advantageous to limit the welding time-periods to an accurate number of few cycles, and to control the welding current through turn-on phase timing. The circuit shown by fig. 5.8.1 permits a fixed-phase synchronous switching with adjustable turn-on phase timing. The triac interrupts the current during the zero-transition at the end of each half-cycle, this way preventing dangerous inductive turn-off voltages. To avoid transformer-remanence, the welding process must always end with a half-cycle opposite the starting one, i. e. for example that a welding process starting with a positive half-cycle must end with a negative half-cycle. Therefore, the control always extends through an even number of half-cycles. If this were not ensured, high turn-on switching currents were liable to occur.

Functional sequence

When the supply voltage is turned on with switch S_1, the integration at network C_1 R_1 causes the RS-flip-flop, made up of two gates of an FZH 191 package, to assume an H-level at its output a. By means of a full-wave rectifier circuit Gl_1 a 100 Hz signal is obtained from the 50 Hz line supply. This signal controls one input of gate 1 through rectifier Gl_2. The second input is already at H. Consequently the output assumes an L-level with each half-cycle, and the counter FZJ 151 as well as the mono-flop FZK 101 are reset and kept at zero.

When the pushbutton is activated, the RS-flip-flop changes state; at its output b an H-signal appears. With each zero-crossing of the line voltage the output of NAND-gate 2 will therefore become L. With the following rise-edge the monoflop FZK 101 is operatad. The inverter in front of gate 2 serves to produce the sharp required. The monoflop output-pulse is differentiated by the C_3 R_3 network and produces with its falling edge a positive control pulse at the output of NAND-gate FZH 201. This pulse is amplified by transistor BCY 58 and fires the triac through a pulse-transformer. The timing of the firing depends on the setting of potentiometer P_1, which in connection with capacitor C_2 determines the length of the monoflop output-pulse. As firing takes place at the back-edge of the pulse, a long pulse means late firing and therefore a low welding current. It should be observed that the timeconstant P_1 C_2 is not made too large, as otherwise the firing pulses might extend into the following half-cycle. The number of firing-pulses supplied is counted by counter FZJ 151. Switch S_2 selects, whether the RS flip-flop is reset after 2, 3, 6,... or 14 firing pulses. Resetting ends the welding cycles. In this way the welding process is always stopped after an even number of cycles, the condition necessary to avoid transformer-remenance problems is met.

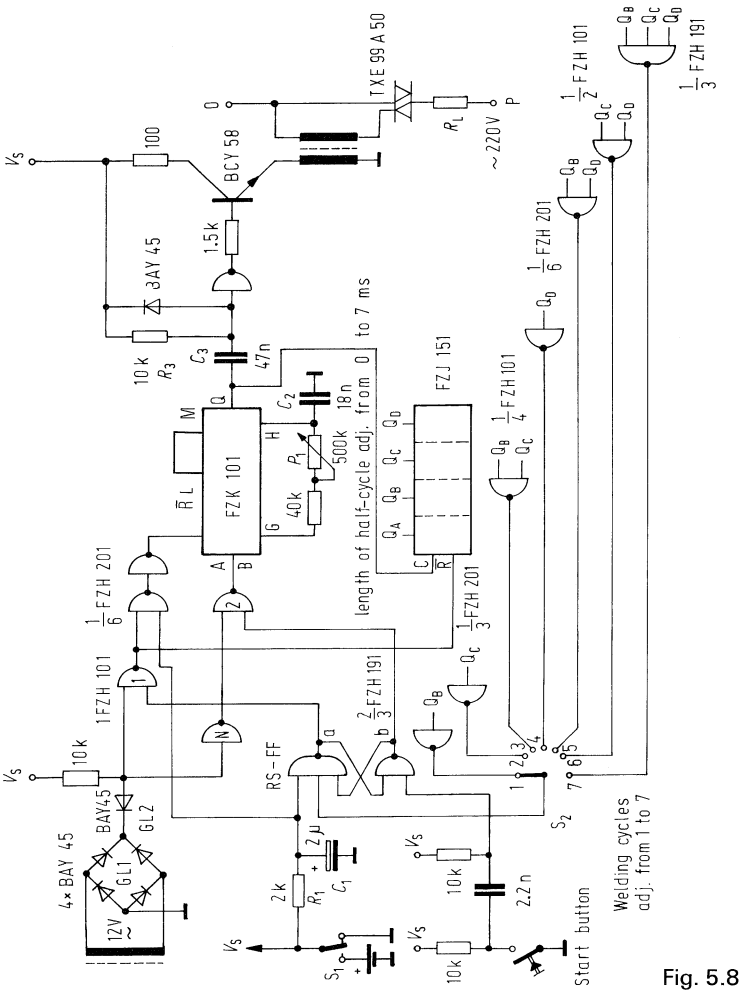

4× BAY 45
12V ~
BAY45
GL1
GL2
10k
1FZH 101
1/6 FZH 201
RS-FF
2/3 FZH 191
1/3 FZH 201
FZK 101
FZJ 151
length of half-cycle adj. from 0 to 7 ms
2k
2 µ
10k
2.2 n
Start button
S1
S2
Welding cycles adj. from 1 to 7
10k
47n
18n
500k
40k
1.5k
100
BCY 58
BAY 45
TXE 99 A 50
~ 220 V
1/4 FZH 101
1/2 FZH 101
1/6 FZH 201
1/3 FZH 191

Fig. 5.8.1

5.8.2 **Motor Control for Touch and Continous Operation**

The motor control circuit to be discussed permits the following modes of operation, initiated by the pushing of keys:

1. continuous right rotation
2. continuous left rotation
3. stop for both directions
4. touch-operation right
5. touch-operation left

During touch-operation the motor will turn only as long as the key is pushed down. This kind of control is used in connection with various tooling-machines, such as adjustment tables, planers etc.
The circuit shown in fig. 5.8.2 has been designed to permit a considerable freedom in the use of the keys. A locking circuit ensures that only one of the two relays for right rotation and left rotation can be activated. It is permissible to immendiately reverse direction. When a change from continuous running to touch-operation is to be made, stop-key 5 must be used first. Even a simultaneous pushing of several keys will not cause any damage. A locking mechanism ensures that the motor can follow one command at a time only.

Functional sequence:

With turn-on of the line voltage both flip-flops are reset by the integrated network R_1/C_1 through the two following gates. If, for example, key 3 for right rotation is depressed next, flip-flop 1 will be set; its output becomes L and therefore the gate output H. A buffer-stage using the Darlington-transistor BDY 88 controls the power relay. To turn it off, the flip-flop is reset. This may be done either by use of the stop-key 5 or key 4 for left rotation. Depressing this key causes relatively quickly, i. e. after two gate propagation delays, the output of gate 1 to change to logic L, whereby the relay starts to become de-energized.
Only then flip-flop 2 will be set with a delay of approx. 20 ms, and gate 2 assumes the output level H. Through the buffer-stage the relay for left rotation begins to pull-in. The delay prevents reliably that both relays might be energized simultaneously, enabling a short-circuit. A realization in such a simple way, with only two additional capacitors, has become possible only through application of the LSL-technique.
When using stop-key 5 both flip-flops are reset, independent of the previous direction of rotation. Consequently gates 3 and 4 are no longer blocked by the output signals of the flip-flops and key 1 or 2 may be used, as desired. The inputs of gates 3 and 4 are H with the exception of one connected to gate 5 or 6, respectively. If this last input becomes H as well, by the use of key 1 or 2, the gate outputs assume an L-level and determine the corresponding direction of rotation through gates 1 and 2 functioning as inverters.

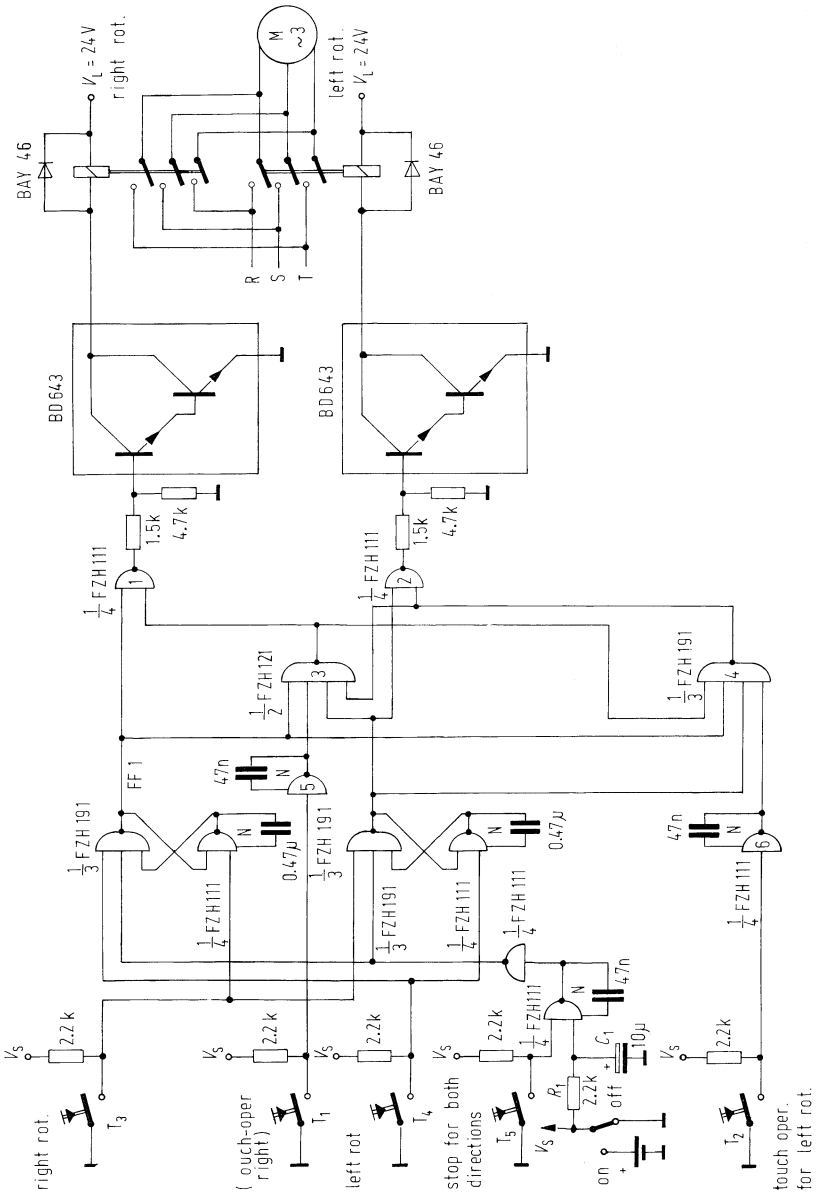

BAY 46
V_L = 24 V
right rot.
M
~3
left rot.
V_L = 24 V
BAY 46
R
S
T
BD643
BD643
1.5k
4.7k
1.5k
4.7k
1/4 FZH111
1/4 FZH111
1/2 FZH121
1/3 FZH191
FF 1
47n
0.47µ
1/3 FZH191
1/3 FZH191
0.47µ
47n
1/4 FZH111
1/4 FZH111
1/4 FZH111
1/4 FZH111
1/4 FZH111
47n
C_1
10µ
P_1
2.2k
V_S
2.2k
V_S
2.2k
V_S
2.2k
V_S
2.2k
V_S
2.2k
V_S
T_3
T_1
T_4
T_5
T_2
right rot.
(ouch-oper right)
left rot
stop for both directions
on
off
touch oper. for left rot.

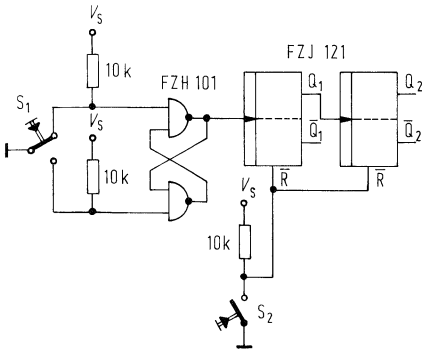
Fig. 5.8.2

5.8.3 **Clocked Rotating Switch Function**

At inputs A, B, C and D logic signals are present which can be switched to the output S sequentially, as would be the case with a rotating switch. Fig. 5.8.3 shows the circuit used. By pushing the key S_2, the circuit may be reset to its initial state (input A connected to S) any time. In the initial state the gate 1 inputs are made up of the signal A and the logic levels of outputs Q_1 and Q_2, both being H. Therefore the output of this NAND-gate depends on signal A. If this signal is L, the gate 1 output will be H and the gate 5 output an L. If the A-signal is an H, the gate 5 output will be H also. The input-information has thus been transferred. When key S_1 is depressed the first flip-flop FZJ 121 will switch with the falling pulse-edge. The two H levels enable the NAND-gate forwarding the information at input B to the output S. Depressing key S_1 once again causes the flip-flops to switch. Gate 3 with Information C becomes enabled. When S_1 is closed again and the first flip-flop has switched, information D is transferred to the output. A further activation of the switch returns the circuit to state A. By using the reset key the initial condition can be restored at any time.

Truth table

	Q_1	$\overline{Q_1}$	Q_2	$\overline{Q_2}$	A	B	C	D	S
I	L	H	L	H	L	–	–	–	L
	L	H	L	H	H	–	–	–	H
II	H	L	L	H	–	L	–	–	L
	H	L	L	H	–	H	–	–	H
III	L	H	H	L	–	–	L	–	L
	L	H	H	L	–	–	H	–	H
IV	H	L	H	L	–	–	–	L	L
	H	L	H	L	–	–	–	H	H



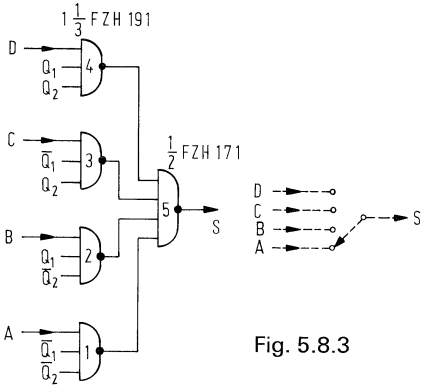


Fig. 5.8.3

5.8.4 **Timelock for Two-hand Control**

Safety circuits of this type are frequently used in tooling machines. For example, they will prevent punch presses from starting operation as long as the hands of the operator are within the danger zone instead of holding on to safety bars outside this zone.
The circuit shown in fig. 5.8.4 produces an output signal when both switches are closed within a certain time limit. It does not matter which switch is closed first or whether they are depressed simultaneously.
Gates 1 and 2 are used as inverters and slowed-down with two externally connected capacitors of 47 nF to make this circuit extremely immune to noise signals. In its resting state the output of gate 5 is at an L level.
When a switch is depressed, one of the two inputs of gate 5 assumes an L-level after the noise-suppression delay has run out, either through path gate 1 gate 2 or through path gate 2 gate 4; the output will switch to a logic H. This triggers the mono-flop FZK 101 and causes it to produce a pulse with a width of 0.28 s. to 3.8 s., depending on the setting of P_1. Therefore one input of gate 6 receives an H. During this time the second input must also be at an H-level for the NAND-requirement to be satisfied. However, the upper input will receive one H-signal only, even if both switches are depressed in any sequence.
Of course, one of the two switches may be a machine-operated contact or a set of logical gates; in these cases it would be required, for example, that within a given time interval after a lamp has lit up, the second switch is closed manually.

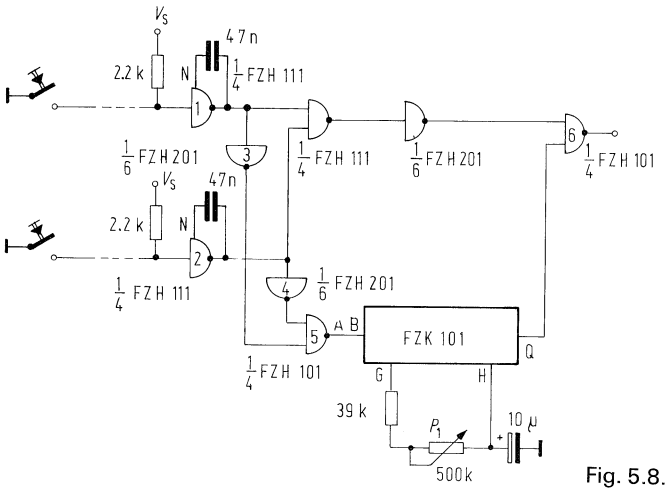


Fig. 5.8.4

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